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MICROWAVE PHOTONICS

Infotonics Technology Center, Inc.

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AIR FORCE RESEARCH LABORATORY
SENSORS DIRECTORATE
ROME RESEARCH SITE
ROME, NEW YORK

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13. ABSTRACT ***(Maximum 200 Words)***

During this program critical infrastructure, technical expertise, and enabling processes necessary to accelerate the development of sensors, alternative power sources and other specific subtopics as well as initiated device development projects of specific interest to DoD were developed. A state-of-the-art microsystems prototype and pilot fabrication facility was established to enable rapid commercialization of new products. With targeted research programs guided by the wealth of expertise of Infotonics' business and scientific staff, enabling technologies and processes were developed to support and accelerate innovative technologies and devices of special interest to the DoD's fume warrior initiative. A flexible, robust multi-user hybrid processing platform for MEMS devices (i.e., waveguides and ROAD-Ms) using Silicon-on-Insulator Wafer was developed to enable the next generation of optoelectronic devices such as optical communication networks, advanced imaging and information sensors and systems, micro-fluidic systems, assembly and packaging technologies and biochemical sensors.

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Executive Summary:

During the grant period **7/9/03 – 9/15/05**, the Infotonics Technology Center developed the critical infrastructure and technical expertise necessary to accelerate the development of sensors, alternative power sources, and other specific subtopics as well as initiated device development projects of specific interest to DOD. Infotonics fosters collaboration among industry, universities and government and operates as a national center of excellence to drive photonics and microsystems development and commercialization. A main goal of the Center is to establish a unique, world-class research and development facility. A state-of-the-art microsystems prototype and pilot fabrication facility was established to enable rapid commercialization of new products. The Center has three primary areas of photonics and microsystems competency: device research and engineering, packaging and assembly, and prototype and pilot-scale fabrication. Center activities focused on next generation optical communication networks, advanced imaging and information sensors and systems, micro-fluidic systems, assembly and packaging technologies, and biochemical sensors. With targeted research programs guided by the wealth of expertise of Infotonics' business and scientific staff, enabling technologies and processes were developed to support and accelerate innovative technologies and devices of special interest to DOD in support of its Future Warrior initiative.

Background:

Photonics, optics, micro-optics, and fiber optics use light to transfer energy and information in order to make possible progressively faster and smaller devices, with wide applicability from medicine to telecommunications. The challenges that face development of such devices are as daunting as their promise. The key enabling technology for next generation products in these markets is the design and fabrication of micro-optical, micro-electrical, and micro-mechanical systems (MOEMS). If the United States is to compete effectively in worldwide markets, it must greatly improve the speed to commercialization of products employing these important emerging technologies. Our university, industrial, and national research laboratories are currently developing the component pieces of photonics and microsystems technology. There is, however, a significant challenge that remains for these enabling technologies—the transition of the technology from the laboratory to the marketplace.

Infotonics is a collaborative, industry led Center of Excellence for applied research & development and commercialization of photonics and microsystems. Formed in 2001 by Eastman Kodak Company, Corning, Inc., and Xerox Corporation, the Center is a not-for-profit corporation which leverages the collective strengths and resources of large and small industries, New York and the U.S government, and over 15 prominent universities. Through our comprehensive infrastructure and extensive industry expertise, Infotonics accelerates the transition from basic and applied research to commercialization of next-generation technologies by reducing financial risk and increasing the probability of commercial success.

Infotonics draws support from the research expertise of our partner educational institutions including; Boston University, Brown University, Columbia University, Cornell University, Rochester Institute of Technology, Syracuse University, University of California, and the University of Rochester. The Rochester Regional Photonics Cluster an association of over 60 small companies dedicated to promoting and enhancing photonics, optics and imaging by fostering cooperation of businesses, academia and government joined Infotonics earlier this year as a small business member.

Infotonics offers the complete capability to move MEMS to market – from design and simulation to a finished packaged device. We have invested more than $15 million in a hybrid silicon-on-insulator

fabrication process that offers significant device flexibility. There are no restrictions to working on just one type of device or in just one product area. We can help build a single prototype, or can scale up to build thousands of devices in pilot production lots. By sharing the Center's prototyping and pilot fabrication facilities for microsystems, cross-industry partners can reduce risks and costs of new product development and accelerate product innovation.

The central objective of the Center, strongly rooted in scientific research, is to promote the commercialization of innovative technologies, guiding them towards widespread commercial products and aerospace applications. Infotonics leverages its considerable capability in MEMs and MOEMs fabrication, optoelectonic packaging and optical testing to design and prototype next generation devices while our basic research and industry partners continue investigations and studies into the next generation of devices.

We provide design services and rapid prototype packaging for photonic, MEMS and microfluidic devices – critical steps during the proof-of-concept development phase. As the project matures, we can do pilot scale manufacturing, developing robust processes that enable an efficient transition to high-volume manufacturing. Infotonics also teamed with our Packaging Alliance partners from the RPI Center for Automation Technologies, and Binghamton University's IEEC for enhanced packaging concept development, reliability, and simulations.

Additional Resources

According to the Cyberstates 4.0 report New York State ranks first in photonics manufacturing. In addition, there is a substantial concentration of photonics and microsystems research & development in New York State, second only to California. This concentration in the upstate New York area and the interaction among the local companies with our member organizations offers fertile ground for collaborative opportunities. Access to a knowledgeable staff and world class shared asset base places a structure and availability to regional research and development efforts in photonics and microsystems here that are not currently present in other regions.

Project Achievements and Accomplishments

1. Facility and tool installation and qualification

1.1 The Foundation Process

When this DOD project was first established, Infotonics was primarily under development with much of its facilities and capabilities still being defined. Early discussions among the founding member companies concluded that the member companies, smaller entrepreneurial companies, and government research and development projects would be best served by the development of a broadly enabling process capability. A benchmark process flow, the Foundation Process, was adopted to guide the choice of processes, and consequently the choice of process tools. This Foundation Process was based upon a Hybrid Silicon-On-Insulator process developed by Xerox as part of a NIST Advanced Technology Program project to overcome design limitations identified with conventional bulk micromachining and material limitations identified with the standard surface-micromachining process. This MOEMS Manufacturing Consortium included Corning IntelliSense, Coventor, Maxim Integrated Products, Microscan Systems, Optical Micro-Machines, Standard MEMS, and Xerox. This hybrid process is based on micromachining an SOI (Silicon-On-Insulator) wafer, which is then used in an add-on polysilicon surface micromachining process after planarization (Fig. 1).

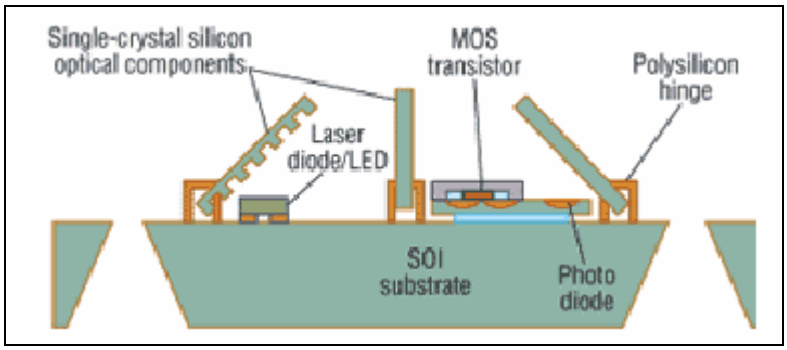


Figure 1. Cross-section of the SOI-based process. SCS optical components have been defined in the device layer of an SOI wafer and rotated out of the plane using hinges defined in polysilicon layers. A laser diode has been integrated using flip-chip bonding,and control and detection electronics have been monolithically integrated into the SCS device layer. (Source: J. Chen, Xerox)

The Single Crystal Silicon (SCS) device layer is used for critical optical and electrical components. The benefits of SCS layers for optical applications have been confirmed by a number of research groups that have used wafer-bonding techniques to incorporate an SCS mechanical layer. By starting with an SOI wafer, this additional wafer-bonding step can be avoided. The SOI device layer has a user-specified thickness that can be selected for a given application, and has excellent, reproducible electrical and mechanical thin-film properties.

By combining a bulk-micromachining SOI process module with a polysilicon surface micromachining module, the design freedom (hinges for out-of-plane components, electrodes) and enhanced manufacturability (anchors to eliminate timed etch and dimples to avoid stiction) enabled by surface micromachining of polysilicon can be coupled with the excellent electrical and mechanical properties of bulk micromachined SCS to obtain the benefits, yet avoid the weaknesses, of these two different

processes. In addition to optical applications, SOI also benefits micro-robots, RF resonators, resonant strain gauges, inertial sensors, and real-time thermal scene simulators.

1.2 Hybrid SOI-MEMS micromachining process

The hybrid SOI-MEMS micromachining process sequence combines bulk and surface micromachining process modules, benefiting from their strengths and avoiding many of their weaknesses. A tetraethyl orthosilicate (TEOS) trench fill and chemical mechanical polishing (CMP) step forms the interface between these two process modules. An overview of the intermediate hybrid process sequence is shown in Fig. 2. The starting SOI wafer is shown in Fig. 2-1. An SOI wafer is used to yield reproducible material properties (Young's modulus, Poisson's ratio), optically flat surfaces, high-Q components, and potentially thick layers that are rigid enough to withstand stresses created by deposited layers.

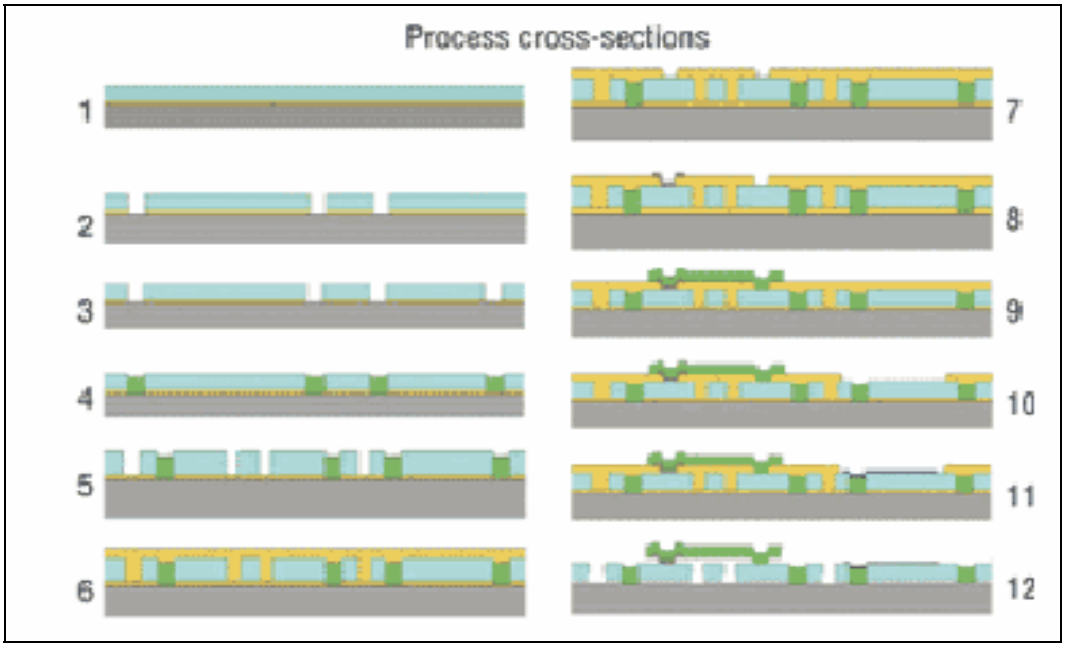


Figure 2. The hybrid SOI micromachining process: 1) SOI wafer; 2) DRIE etches through the SCS layer for anchors and dimples; 3) timed etch of buried oxide layer for the formation of dimples; 4) polysilicon deposition and blanket etch back to anchor released SCS components to the handle wafer, and to form polysilicon dimples; 5) DRIE through the SCS layer to form released SCS components; 6) TEOS fill and CMP; 7) anchors to the SCS layer; 8) dielectric isolation; 9) polysilicon structures; 10) windows down to the SCS layer for mirrors that are to be metallized; 11) metallization; and 12) sacrificial release (wet or dry). (Source: P. Gulvin, Xerox)

Holes are etched into the active silicon (Fig. 2-2) and into or through the buried oxide below (Fig. 2-3), and then are refilled with polysilicon (Fig. 2-4). If the buried oxide is completely removed, then the polysilicon acts as an anchor to the substrate. If the buried oxide is only partially removed, then the polysilicon forms a protrusion from the bottom of the active silicon that acts as a dimple for preventing stiction, as is seen in standard surface-micromachining processes. Holes are etched into the silicon to form the desired silicon structures (Fig. 2-5). The wafer is then planarized with a TEOS deposition and CMP to eliminate large topography that would make further lithography difficult (Fig. 2-6).

The process sequence then switches to a purely surface-micromachining process module. Vias to the silicon layer are etched to allow subsequent layers to anchor (Fig. 2-7). Silicon nitride is deposited to allow electrical isolation (Fig. 2-8). Polysilicon is deposited to form tops of hinges, electrode plates, caps for tops of sliders, and bridges for traces (Fig. 2-9). Additional holes to the silicon are created (Fig. 2-10), and metal is deposited to form the traces and bond pads, and to act as the reflective surface on mirrors (Fig. 2-11).

The wafers are then diced, sorted, and shipped to the user for release (Fig. 2-12). By using this hybrid combination of bulk and surface-micromachining modules, all of the strengths listed previously are combined, and most of the weaknesses are mitigated.

1.3 Microfabrication Facility Planning and Renovation

The choice of the Foundation Process then drove Infotonics' initial choices of process tools and processes. In addition to the processes required by the Foundation Process Flow, additional processes were included to meet other member company requirements and to provide some processes not yet requested, but expected to be of broad interest to future customers. These groups of processes are listed in Fig. 3 along with SEM photos of examples of the types of devices representing each group.

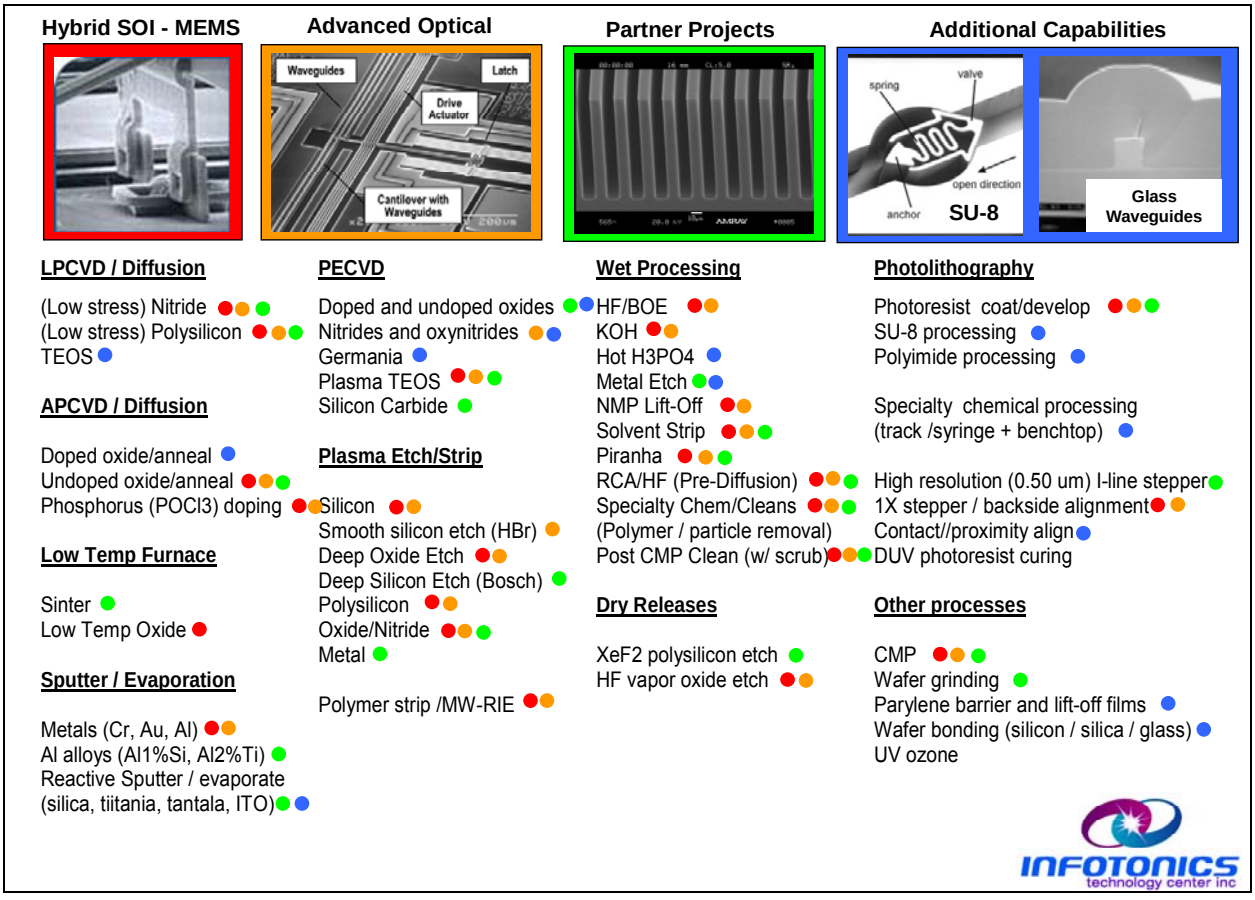


Figure 3. Infotonics' microfabrication process capabilities. In this figure processes highlighted in red are those required by the hybrid SOI or Foundation process. Those highlighted in orange are used by an extension of the Foundation Process, the Advanced Optical Process which enables the integration

of silicon optical waveguides with MEMS. Finally the green- and blue-highlighted processes are those additional processes required by other member companies and for a broad-based capability respectively.

As technical staff were added in 2003 the design of the microfabrication facility proceeded based on the desired processes described above. DOD funds helped support the technical staff during planning and buildout of the facility, tool selection and installation, and process development. Facility design and process tool evaluation and purchasing took place in parallel. Infotonics contracted the services of an architectural firm, Pathfinder, Inc., and a general contractor, LeChase Construction, to bring up the facility. Weekly meetings were held between the technical staff and the architect to update the facility layout. Daily meetings were conducted with the contractor to follow progress on demolition and facility renovation, and eventually during tool placement, on progress on tools. A rough schedule for the tasks involved in bringing up the microfabrication facility is shown in Figure 4.

Based on the processes required for the Foundation Process, the engineering staff could define the equipment. 109 tools had to be selected. For each tool quotes were solicited from three vendors and a selection was made based on a tool comparison sheet. Table 1 is an example of the sheet used in the selection of one of the 109 tools, the ULVAC Enviro photoresist stripper.

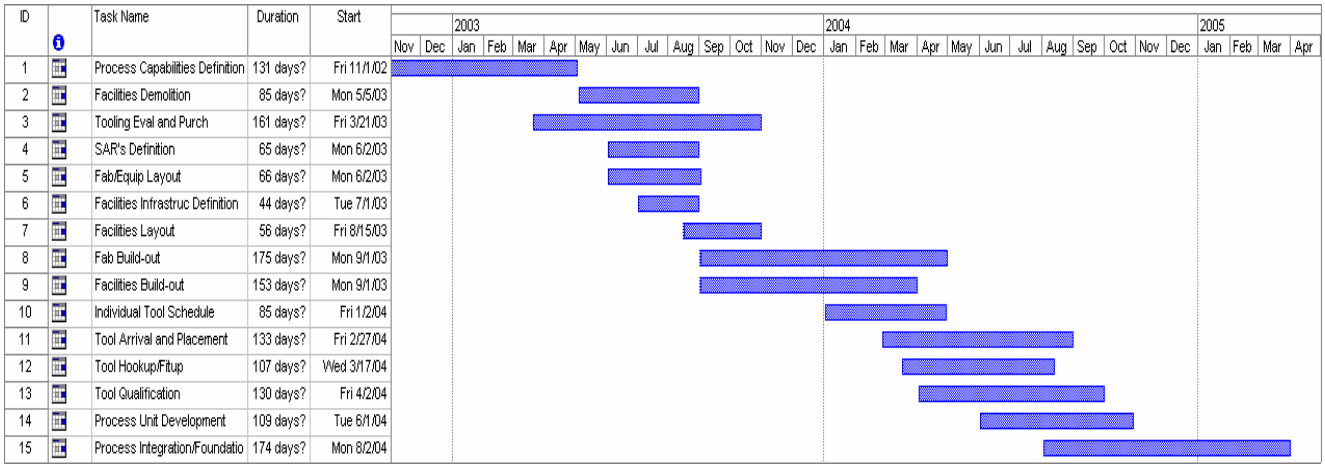


Figure 4. Infotonics Technology Center Build-out Schedule

October 16,2003		Resist/Residue Removal System Comparison		
Vendor Evaluation	Mary Winters			
Equipment:	Resist/Residue Removal System			
	Criteria	ULVAC ENVIRO	MATRIX	NOVELLUS
Hardware Requirements	6" Si Wafer Capable	0	0	0
	8" Si Wafer Capable	0	0	0
	6" Quartz wafers	0	0	0
	Microwave and RIE capability	0	0	0
	Load-lock capability	0	0	0
	Wafer Temperature Control	0	0	0
	End-Point Detection	0	0	0
	Sapphire applicator kit	0	0	0
	Pumps supplied by Infotonics	0	0	0
Process Requirements	Process flexibility	0	0	0
	Deveil process	0	0	0
	Residue Removal	0	0	0
	Capability to release sacrificial layers	0	0	0
	Polyimide removal	0	0	0
	Capability to deposit CFx polymer films	+	-	-
	Bulk Ash Removal Rate	-	0	+
	Particulates	0	0	0
	Gases: NF3, H2-N2, CF4, O2,Ar	0	0	0
	Uniformity (within wafer) <5%	-	+	+
Support	90% Equipment Uptime	0	0	0
	Process Engineering Support	0	0	0
	Field Service Support	+	0	0
Experience	MEMS Experience	+	0	0
Facilities	Ease of facilitation (Facility Prep Document)	0	0	0
	Is there any ancillary equipment not included in the quote (pumps, chiller)	0	0	0
	Drawings of footprint of equipment (including ancillary equipment)	0	0	0

Terms	Warranty (Parts and Labor Included)	0	0	0
	6 month warranty length	0	+	-
Maintenance	Is the system configured for easy access	0	0	0
	Telephone response	+	0	0
	Response Time	+	0	0
	Spare Parts Availability	0	0	0
	Service Engineer Location	+	0	0
Qualification	Hardware Qualification	0	0	0
	Process Qualification	0	0	0
Training	On-site	0	0	0
	At Factory	0	0	0
Pricing	Price Advantage	+	-	-
Cost	Base Price	$290,000	380,000	$500,000
	Options	$68,759	$95,900	$0
	6 month warranty	Inc	2 yr.	3 mo
	Extended warranty (covering 12 months)	$24,000	$0	$86,475
	Total Cost	$382,759	$475,900	$586,475
Additional Comments	Matrix was recently bought out by Axcelis Pumps will be supplied by Infotonics			
Conclusion	Total +	7	2	2
	Total -	2	2	3

Table 1. Tool comparison checklist for ULVAC photoresist stripper

Once tools were selected, the SARS, or Schedule of Area Requirements Sheet, could be prepared. Process gas and facility requirements were established by each engineer for his or her process tools. For example, Table 2 shows the process gases required by the dry, or plasma, etch tools. The SARS summarizes the expected process chemical, process gas, electrical power, etc., required by all the tools based on these engineering requirements and estimates of the number of wafers to be processed using these processes. The physical layout of the tools and the facilities connections drove the fab layout and the SARS estimates drove the layout of the process and support gas supply lines. Appendix A is an extract from the SARS showing the rollup of the estimated chemical usage and process gas usage, as well as a tool / gas usage matrix. The final microfabrication facility layout is shown in Fig. 5. As is stated elsewhere, the microfabrication facility, or “fab”, is a 23,000 sq. ft. bay and chase cleanroom with just under 10,000 sq. ft. Class 100. The layout shows the bay and chase design of the facility. The process tools, the red and orange figures in the layout, are bulkheaded through the walls of the bays, with the

silicon wafer handling done inside the bays and the support equipment (pumps, water lines, gas lines, etc.) outside in the chase.

Dry Etch
Gases

STS				
70-E05	70-E04	50-F06	70-E08	50-F14
ASE	AOE	PECVD	ASE-PRO	PECVD - PRO
C4F8	C4F8	N2	C4F8	N2
SF6	SF6	O2	SF6	O2
O2	O2	C4F8	O2	C4F8
Ar	CO2	N2O	Ar	N2O
	He	Ar		Ar
	H2	CH4		CH4
	CF4	SiH4		SiH4
		2%Ge4/Ar		NH3
		5%Ph2/N2		
		5%B2H6/H2		
		NH3		
He	He		He	
N2	N2	N2	N2	N2

LAM			
50-E03B	50-E03S	50-E03M	50-E03L
Dieletric	Poly	Metal	MS
	O2	N2	N2
O2	CF4	O2	O2
CF4	SF6	SF6	
C4F8	He	Ar	
SF6	Ar	Cl2	
Ar	Cl2	BCl3	
CHF3	HBr		
	CHF3		
	N2		
He	He	He	
N2	N2	N2	N2
			H2O Vapor

PlasmaTherm
60-E07
SF6
CHF3
O2
NF3

ULVAC
70-E06
O2
NF3
CF4
N2-H2
Ar

Table 2. Dry Etch Tool Gas Requirements

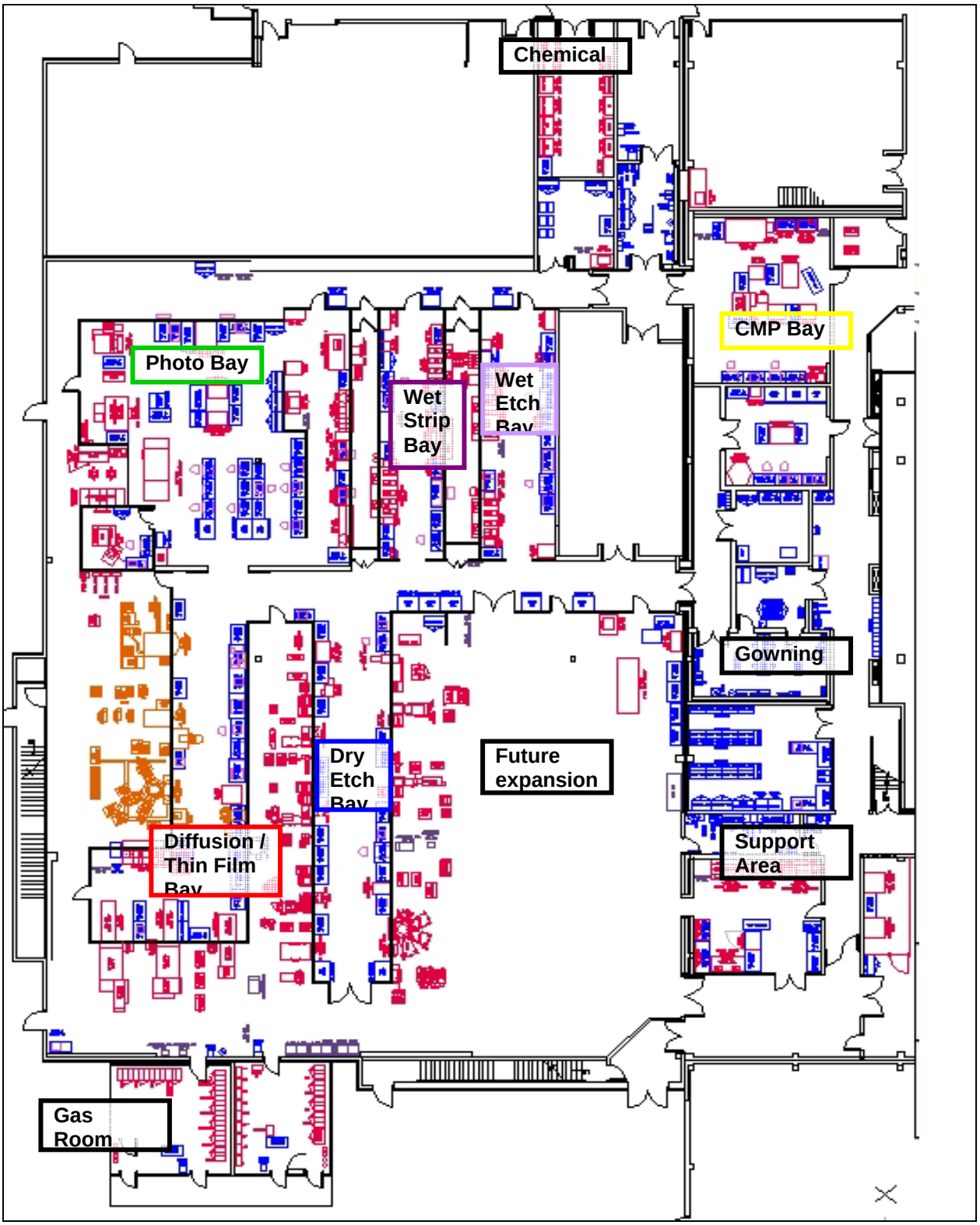


Figure 5. Infotonics Technology Center cleanroom layout

Once the cleanroom was complete, the staff proceeded with tool installation. First, a schedule was established for tool installation. A detailed installation schedule for the ULVAC is shown in Fig. 6 to illustrate the processes involved in tool installation. A commissioning check list was drawn up specifically for each tool to ensure proper facilitization and that all process performance conditions were met. The commissioning checklist for the ULVAC resist stripper is shown in Appendix B. The installation of tools were coordinated in order to avoid resource conflicts while maximizing the use of the engineering staff. The overall tool schedule is shown in Fig. 7.

ID	Proc_Area	Priority	Order	Task Name	Tool_ID	Source	Contact
946	**Etch**	**640**	**0**	**O2 Plasma/RIE (Strip) Ul**	**70-E06**	**Ulvac**	**MW**
947	Etch	640	0	Tool Selection	70-E06		MW
948	Etch	640	0	PO Placed	70-E06		MW
949	Etch	640	0	Vendor Lead Time	70-E06		MW
950	Etch	640	0	Fit-Up Documents Subr	70-E06		MW
951	Etch	640	0	Ship	70-E06		MW
952	Etch	640	0	Received from Vendor	70-E06		MW
953	Etch	640	0	Prep	70-E06		MW
954	Etch	640	0	Place in Fab	70-E06		MW
955	Etch	640	0	Facilitization	70-E06		MW
956	Etch	640	0	Wafers avail for qual	70-E06		MW
957		500	0	NF3			
958	Etch	640	0	Equip Startup/Prove-In	70-E06		MW
959	Etch	640	0	Metrology Avail	70-E06		MW
960	**Etch**	**640**	**0**	**Process Qual**	**70-E06**		**MW**
961	Etch	640	0	Resist Strip	70-E06		MW
962	Etch	640	0	Training	70-E06		MW
963	Etch	640	0	Prepare Documentatior	70-E06		MW
964	Etch	640	0	Tool Ready	70-E06		MW

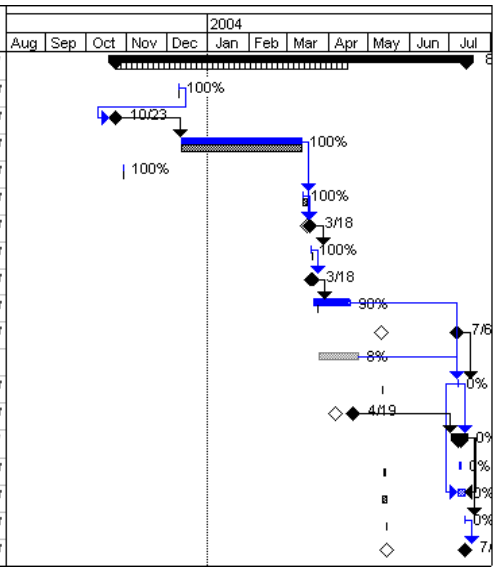
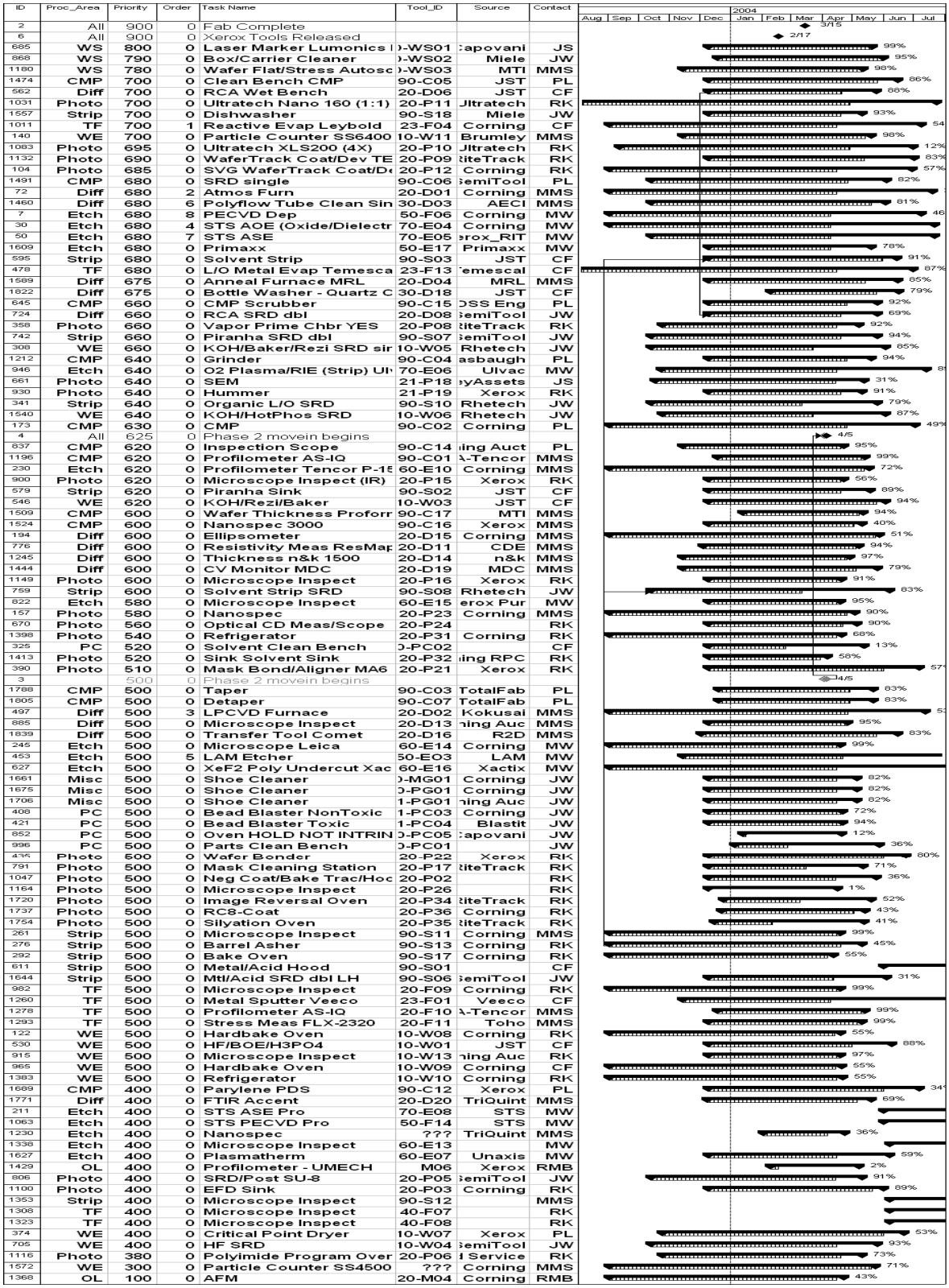


Figure 6. Tool Installation Schedule Detail for ULVAC.



ID	Proc_Area	Priority	Order	Task Name	Tool_ID	Source	Contact
2	All	900	0	Fab Complete			
6	All	900	0	Xerox Tools Released			
685	WS	800	0	Laser Marker Lumonics J	)-WS01	apovani	JS
868	WS	790	0	Box/Carrier Cleaner	)-WS02	Miele	JW
1180	WS	780	0	Wafer Flat/Stress Autosc	)-WS03	MTI	MMS
1474	CMP	700	0	Clean Bench CMP	90-C05	JST	PL
562	Diff	700	0	RCA Wet Bench	20-D06	JST	CF
1031	Photo	700	0	Ultratech Nano 160 (1:1)	20-P11	Ultratech	RK
1557	Strip	700	0	Dishwasher	90-S18	Miele	JW
1011	TF	700	1	Reactive Evap Leybold	23-F04	Corning	CF
140	WE	700	0	Particle Counter SS6400	10-W11	Brumley	MMS
1083	Photo	695	0	Ultratech XLS200 (4X)	20-P10	Ultratech	RK
1132	Photo	690	0	WaferTrack Coat/Dev TE	20-P09	iteTrack	RK
104	Photo	685	0	SVG WaferTrack Coat/D	20-P12	Corning	RK
1491	CMP	680	0	SRD single	90-C06	emiTool	PL
72	Diff	680	2	Atmos Furn	20-D01	Corning	MMS
1460	Diff	680	6	Polyflow Tube Clean Sin	30-D03	AECI	MMS
7	Etch	680	8	PECVD Dep	50-F06	Corning	MW
30	Etch	680	4	STS AOE (Oxide/Dielectr	70-E04	Corning	MW
50	Etch	680	7	STS ASE	70-E05	rox_RIT	MW
1609	Etch	680	0	Primaxx	50-E17	Primaxx	MW
595	Strip	680	0	Solvent Strip	90-S03	JST	CF
478	TF	680	0	L/O Metal Evap Temesca	23-F13	emescal	CF
1589	Diff	675	0	Anneal Furnace MRL	20-D04	MRL	MMS
1622	Diff	675	0	Bottle Washer - Quartz C	30-D18	JST	CF
845	CMP	660	0	CMP Scrubber	90-C15	DSS Eng	PL
724	Diff	660	0	RCA SRD dbl	20-D08	emiTool	JW
358	Photo	660	0	Vapor Prime Chbr YES	20-P08	iteTrack	RK
742	Strip	660	0	Piranha SRD dbl	90-S07	emiTool	JW
308	WE	660	0	KOH/Baker/Rezi SRD sir	10-W05	Rhetech	JW
1212	CMP	640	0	Grinder	90-C04	asbaugh	PL
946	Etch	640	0	O2 Plasma/RIE (Strip) UI	70-E06	Ulvac	MW
661	Photo	640	0	SEM	21-P18	yAssets	JS
930	Photo	640	0	Hummer	21-P19	Xerox	RK
341	Strip	640	0	Organic L/O SRD	90-S10	Rhetech	JW
1540	WE	640	0	KOH/HotPhos SRD	10-W06	Rhetech	JW
173	CMP	630	0	CMP	90-C02	Corning	PL
4	All	625	0	Phase 2 movein begins			
837	CMP	620	0	Inspection Scope	90-C14	ing Auct	PL
1196	CMP	620	0	Profilometer AS-IQ	90-C01	-Tencor	MMS
230	Etch	620	0	Profilometer Tencor P-1	60-E10	Corning	MMS
900	Photo	620	0	Microscope Inspect (IR)	20-P15	Xerox	RK
579	Strip	620	0	Piranha Sink	90-S02	JST	CF
546	WE	620	0	KOH/Rezi/Baker	10-W03	JST	CF
1509	CMP	600	0	Wafer Thickness Proforr	90-C17	MTI	MMS
1524	CMP	600	0	Nanospec 3000	90-C16	Xerox	MMS
194	Diff	600	0	Ellipsometer	20-D15	Corning	MMS
776	Diff	600	0	Resistivity Meas ResMap	20-D11	CDE	MMS
1245	Diff	600	0	Thickness n&k 1500	20-D14	n&k	MMS
1444	Diff	600	0	CV Monitor MDC	20-D19	MDC	MMS
1149	Photo	600	0	Microscope Inspect	20-P16	Xerox	RK
759	Strip	600	0	Solvent Strip SRD	90-S08	Rhetech	JW
822	Etch	580	0	Microscope Inspect	60-E15	erox Pur	MW
157	Photo	580	0	Nanospec	20-P23	Corning	MMS
670	Photo	560	0	Optical CD Meas/Scope	20-P24		RK
1398	Photo	540	0	Refrigerator	20-P31	Corning	RK
325	PC	520	0	Solvent Clean Bench	)-PC02		CF
1413	Photo	520	0	Sink Solvent Sink	20-P32	ing RPC	RK
390	Photo	510	0	Mask Bond/Aligner MA6	20-P21	Xerox	RK
3		500	0	Phase 2 movein begins			
1788	CMP	500	0	Taper	90-C03	TotalFab	PL
1805	CMP	500	0	Detaper	90-C07	TotalFab	PL
497	Diff	500	3	LPCVD Furnace	20-D02	Kokusai	MMS
885	Diff	500	0	Microscope Inspect	20-D13	ing Auc	MMS
1839	Diff	500	0	Transfer Tool Comet	20-D16	R2D	MMS
245	Etch	500	0	Microscope Leica	60-E14	Corning	MW
453	Etch	500	5	LAM Etcher	50-EO3	LAM	MW
627	Etch	500	0	XeF2 Poly Undercut Xac	60-E16	Xactix	MW
1661	Misc	500	0	Shoe Cleaner	)-MG01	Corning	JW
1675	Misc	500	0	Shoe Cleaner	)-PG01	Corning	JW
1706	Misc	500	0	Shoe Cleaner	1-PG01	ing Auc	JW
408	PC	500	0	Bead Blaster NonToxic	1-PC03	Corning	JW
421	PC	500	0	Bead Blaster Toxic	1-PC04	Blastit	JW
852	PC	500	0	Oven HOLD NOT INTRIN	)-PC05	apovani	JW
996	PC	500	0	Parts Clean Bench	)-PC01		JW
438	Photo	500	0	Wafer Bonder	20-P22	Xerox	RK
791	Photo	500	0	Mask Cleaning Station	20-P17	iteTrack	RK
1047	Photo	500	0	Neg Coat/Bake Trac/Hoc	20-P02		RK
1164	Photo	500	0	Microscope Inspect	20-P26		RK
1720	Photo	500	0	Image Reversal Oven	20-P34	iteTrack	RK
1737	Photo	500	0	RC8-Coat	20-P36	Corning	RK
1754	Photo	500	0	Silyation Oven	20-P35	iteTrack	RK
261	Strip	500	0	Microscope Inspect	90-S11	Corning	MMS
276	Strip	500	0	Barrel Asher	90-S13	Corning	RK
292	Strip	500	0	Bake Oven	90-S17	Corning	RK
611	Strip	500	0	Metal/Acid Hood	90-S01		CF
1644	Strip	500	0	Mtl/Acid SRD dbl LH	90-S06	emiTool	JW
982	TF	500	0	Microscope Inspect	20-F09	Corning	RK
1260	TF	500	0	Metal Sputter Veeco	23-F01	Veeco	CF
1278	TF	500	0	Profilometer AS-IQ	20-F10	-Tencor	MMS
1293	TF	500	0	Stress Meas FLX-2320	20-F11	Toho	MMS
122	WE	500	0	Hardbake Oven	10-W08	Corning	RK
530	WE	500	0	HF/BOE/H3PO4	10-W01	JST	CF
915	WE	500	0	Microscope Inspect	10-W13	ing Auc	RK
965	WE	500	0	Hardbake Oven	10-W09	Corning	CF
1383	WE	500	0	Refrigerator	10-W10	Corning	RK
1689	CMP	400	0	Parylene PDS	90-C12	Xerox	PL
1771	Diff	400	0	FTIR Accent	20-D20	TriQuint	MMS
211	Etch	400	0	STS ASE Pro	70-E08	STS	MW
1063	Etch	400	0	STS PECVD Pro	50-F14	STS	MW
1230	Etch	400	0	Nanospec	???	TriQuint	MMS
1338	Etch	400	0	Microscope Inspect	60-E13		MW
1627	Etch	400	0	Plasmatherm	60-E07	Unaxis	MW
1429	OL	400	0	Profilometer - UMECH	M06	Xerox	RMB
806	Photo	400	0	SRD/Post SU-8	20-P05	emiTool	JW
1100	Photo	400	0	EFD Sink	20-P03	Corning	RK
1353	Strip	400	0	Microscope Inspect	90-S12		MMS
1308	TF	400	0	Microscope Inspect	40-F07		RK
1323	TF	400	0	Microscope Inspect	40-F08		RK
374	WE	400	0	Critical Point Dryer	10-W07	Xerox	PL
705	WE	400	0	HF SRD	10-W04	emiTool	JW
1116	Photo	380	0	Polyimide Program Over	20-P06	Service	RK
1572	WE	300	0	Particle Counter SS4500	???	Corning	MMS
1368	OL	100	0	AFM	20-M04	Corning	RMB

Figure 7. Tool Installation Schedule

During the first three quarters of 2004, as the facility renovation was completed, tool installation and process qualification proceeded in parallel. Each tool had a set of processes, previously agreed upon with the vendor, that had to be run to specification before the tool could be formally accepted by Infotonics. An example of the tool acceptance authorization, again for the ULVAC is included in Appendix C. Most of the tool qualification processes were those required for the Foundation Process and other project processes that had been identified. The processes and tools finally supported by the facility are listed in Table 3.

Photo Processes

PR thickness (um)	Resist
.65	1075HiR
1.8	906-17
2.5	906-17
7	SPR220-7
7.5	AZ2070

Exposure Tools	Type	Alignment	Resolution *	Front/Back Align?
U/T XLS200 4X Stepper	Projection	+/-.15um	0.5um	N
U/T Nano160 1X Stepper	Projection	+/-.25um	2um	Y (+/- 2um)
MA6 Karl Suss	Contact/Prox	+/-3um	2um	Y

*Note: depends on resist thickness (stated for 1.8um PR thickness)

Diffusion/Furnace Operations

Film	Thickness	Uniformity	Stress	Temp (C)
Wet Thermal Oxide	5000-40000A		NA	1100-1200
N2 Anneal	NA		NA	900-1250
Dry Thermal Oxide	300-4000A		NA	1000-1100
POCl3 Diffusion		depends on Rs	NA	900-1100
LPCVD TEOS	500 - 10,000A	< 5%	NA	700
Si3N4	500 - 10,000A	< 2.5%	~ 900 Mpa	800
Low Stress SixNy	500 - 20,000A	< 5%	< 300 MPa	810
Polysilicon	500 - 30,000A	< 2.5%	-400 -200 MPa	625
a-Si	500 - 30,000A	< 4%	200-400 MPa	565
N2 Anneal	NA	NA	NA	350- 750
3% H2/N2 Anneal	NA	NA	NA	350- 750

Plasma Enhanced Chemical Vapor Deposition (PECVD)

Films	Thickness Range Tool	Uniformity	Stress	Aspect Ratio (Gapfill)
TEOS (compressive)	1000A to 7um Gapfill (1:1)	<3% STS	<350MPa	
Silicon Nitride (compressive or tensile)	1000A to 2 um	<2% STS	<100MPa	
Silicon Dioxide	1000A to 2um	<2%	<300MPa	

CMP

Film	Thickest Film	Uniformity	Particle Counts	Tool
Oxide	8um	<4%	<200 @.2um+	Strasbaugh 6EC
Silicon		TTV <5%	<200 @.2um+	Strasbaugh 6EC
Grind (Silicon)	Thin to 300um	TTV <5%	Bow/Warp<50um	Strasbaugh 7IIA

Physical Vapor Deposition

Veeco Connexion 800 Sputter	Temescal FCE 2700A Evaporator	Leybold APS 1104 (Reactive) Evaporator
(Single wafer)	(Metals – Dome + Planetary)	Optical Films (Filmstacks)
Al	Ni	HfO_2
Al/1% Si	Cr	SiO_2
ITO	Au	
Mo	Al	
Ta	Sn	
Al/Nd	Ti	
Ti		
TiW		

(Specific thickness and measured stress information is available upon request).

Dry Etch

Film	E/R	Selectivity (to resist)	Unif.	Tool
Nitride	5000A/min	3:1	<5%	LAM 4520XLe
Oxide	7800A/min	6:1	<5%	LAM 4520XLe
Undoped poly	2200A/min	3:1	<5%	LAM 9400
Aluminum	9000A/min	------	<5%	LAM 9600
Photoresist	3um/min	------	<5%	Ulvac Enviro
DRIE Si	2-3um/min	100:1	<3%	STS ASE (Standard Rate)
DRIE Oxide	1000A-10um	7:1	<3%	STS AOE

Wet Chemistries

Wet Etch	Chemistry	Temp (C)	Etch Rate
Aluminum Etch	16:1:1:2 (Phosphoric, Nitric, Acetic, Water)	40	4000 A/min
KOH (Si V-Groove)	25%	80	1um/min
BOE (Oxide Etch)	6:1:1 (Water: HF:NH4F)	30	1300 A/min
Hot Phosphoric/Nitride (thermal)	Concentrated Phosphoric Acid	160	40 A/min
HF (Dip)	10:1 (HF:Water)	ambient	

Clean/Wet Strip/Lift-Off	Chemistry	Temp (C)
RCA1 (Diff Cln)	10:2:1 Water:Peroxide:Ammonium Hydroxide	50
RCA2 (Diff Cln)	10:2:1 Water:Peroxide:Hydrochloric	50
Piranha	1:4 Peroxide: Sulfuric Acid	110
Solvent Strip	EKC 265	70
Lift-Off Solvent – NMP	NMP	75

Metrology	
Property	**Tool**
Profiles, CDs, SEM inspection	SEM Hitachi 4700 Cold Cathode FE
Surface roughness, profiles	AFM (Quesant QScope 350)
Oxide quality	CV Monitor CSM/Win-TVS/1 (MDC)
Thin Film Thickness, RI	Ellipsometer (Rudolph)
B, P in BPSG; C, O in Si, SOI thickness	FTIR QS-2200A (Accent)
Thin Film Thickness	Nanospec 210 (Nanometrics)
Critical Dimensions	Nikon L-200 (Brook-ANCO)
Particles	Particle Counter 6420 (KLA-Tencor)
Dynamic Profilometer	Profilometer – UMECH (ETEC)
Step Height	Profilometer AS-IQ (KLA-Tencor)
Step Height/Profilometer	Profilometer P-15 (KLA -Tencor)
Film/Wafer resistance	Resistivity Meas ResMap 168 (CDE)
Thin Film Stress	FLEX 2320 (Toho)
Thin Film thickness, RI, Reflectance	Thickness n&k 1500 (n&k)
Wafer Flatness/Stress	Wafer Flat/Stress Autoscan 200 (MTI)
Wafer Thickness	Wafer Thickness Proforma 300 (MTI)

Table 3. Infotonics' Supported Processes

2. Process Integration: Foundation Process Development at Infotonics

As tool installation and unit process qualification came to a close, attention turned towards process integration of the Foundation Process. The Foundation Process would be the basis of the second year microfabrication projects for the DOD contract: Silicon Optical Waveguides and the Reconfigurable Optical Add-Drop Multiplexer (R-OADM). As described earlier, the Foundation Process was derived from a NIST-funded Advanced Technology Program project to develop a Hybrid SOI process. During the course of the ATP project the process had been transferred to two Si MEMS wafer fabs, Standard MEMS and Corning IntelliSense. Each fab had run through the basic 8 mask process (not including the Advanced Optical module for waveguides) a couple of times each before economic conditions forced the closure of each company. Corning IntelliSense, as part of the Infotonics founding member company, Corning, Inc. was able to share with Infotonics some of the lessons learned and outstanding process problems on the Foundation Process.

The main process issues which had to be addressed by Infotonics' technical staff in bringing up the Foundation Process were:

1) SCS layer doping
2) Anchor and Dimple via etch profiles
3) Polysilicon fill and planarization
4) TEOS gap fill process.
5) CMP oxide planarization
6) Low stress nitride and polysilicon

Each of these will be addressed in turn.

2.1 SCS layer doping.

The original ATP process used a phosphorus implant which was outsourced to Implant Services, Inc., and used a single doping concentration, 10 Ohm/sq., enough to permit low current conduction sufficient for capacitors and for a groundplane. Infotonics needed to develop a furnace-based POCl3 doping process to utilize its in-house diffusion capabilities. Also, because of the addition of the Advanced Optical Module which incorporated higher-current thermal actuators than had been used in the ATP process, an additional 3 Ohm/sq. doping capability was required.

2.2 Anchor and Dimple etch via profiles.

The shape of the Anchor and Dimple etched vias are important. These vias are subsequently filled with polysilicon and provide a mechanical connection between the final released MEMS structure and the silicon substrate. Fig. 8 shows the desired slightly sloped profile.

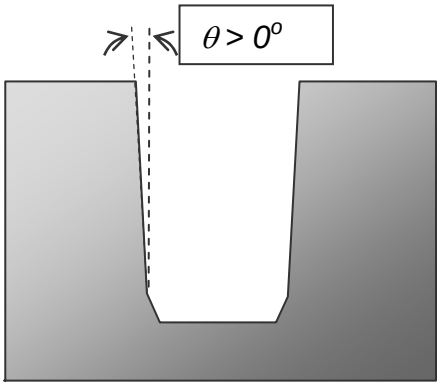


Figure 8. Desired profile of the Anchor Via

If the walls are too sloped, the via is not filled and cannot subsequently be planarized (Fig. 9). If the via walls are too steep, the LPCVD polysilicon deposition will pinch off the via before it is filled, leaving a void or "keyhole" in the via (Fig. 10). When these vias are planarized, the keyhole can fill with CMP (chemical-mechaical polish) slurry. This residue is difficult to clean and leads to contamination of the wafers. The process initially was developed at IntelliSense for ATP with too large a slope and were not planarizable (Fig. 9). They developed their etch process to the point where the vias were steeper, but exhibited the pinch-off in the polysilicon (Fig. 10) with the subsequent keyhole.

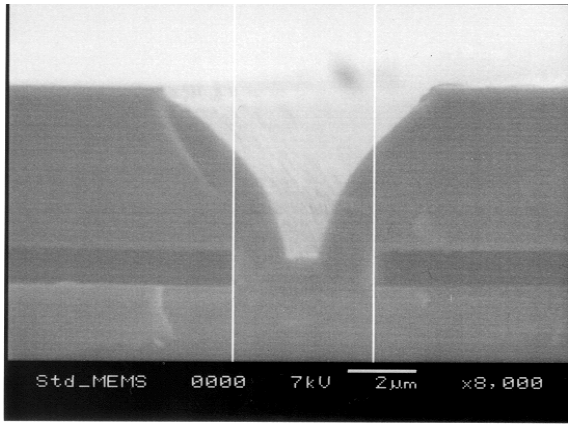


Figure 9. Initial Anchor Vias from ATP Program. Note wide vias and poor planarization

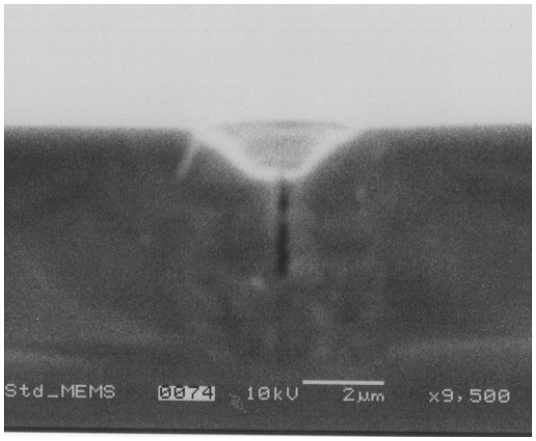


Figure 10. Final Anchor Vias from ATP Program. Note exposed keyhole and poor planarization

Infotonics ran a Design of Experiments on the silicon etch process and between our two etch tools, the STS Advanced Silicon Etcher and the LAM 9400 Polysilicon Etcher to control the via profile. A process was developed that provided the correct slope to permit a keyhole free polysilicon fill. (Fig. 11).

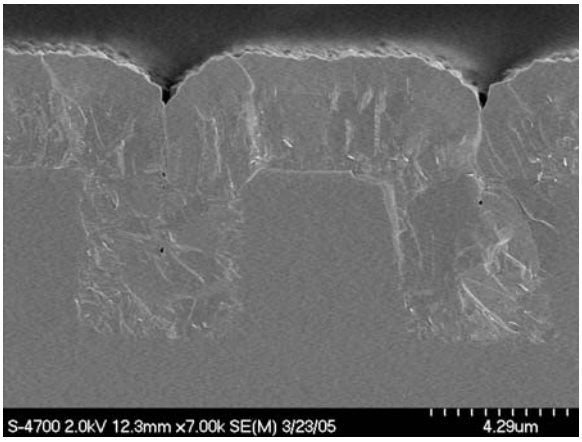


Figure 11. Anchor vias with keyhole free polysilicon fill using ITC's process

2.3 Polysilicon Etchback Planarization.

When the ATP polysilicon etch-back approach was used to planarize the polysilicon in the vias, the etch preferentially attacked the seam in the center of the via (Fig. 12). An approach was developed to eliminate the crack by first oxidizing the surface of the polysilicon. The oxidation smoothed out the polysilicon topography (Fig. 13), and a subsequent oxide strip provides a more planar starting surface for the etchback (Fig. 14).

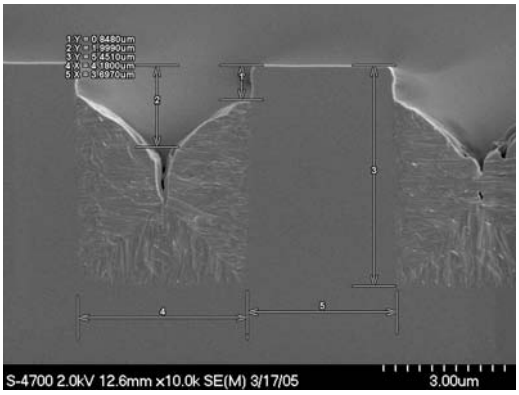


Figure 12. Attack of polysilicon fill during etchback

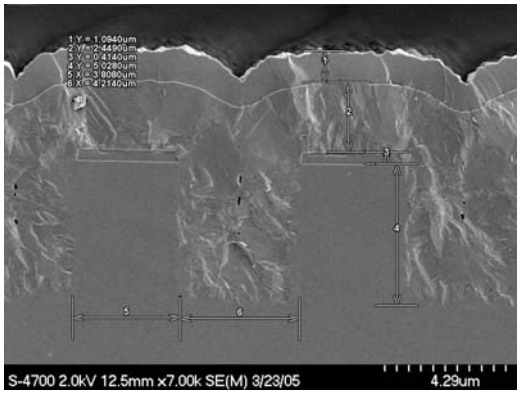


Figure 13. Smoothing of the polysilicon by oxidation

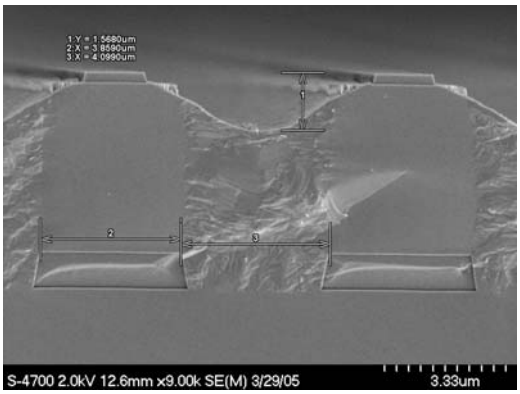


Figure 14. Anchor via after polysilicon fill, oxidation, and planarization. Note gentle profile and lack of keyhole.

2.4. TEOS Gapfill and Planarization Process.

The interface between the single crystal silicon "bulk" micromachining modules and the surface micromachined polysilicon and nitride levels is the Planar Oxide. The purpose of this layer is to planarize the deep topography of the SCS layer, which consists of features up to 6 um deep with widths of 3 um to many microns, and provide a level surface upon which to fabricate polysilicon mechanical structures and metal electrical leads. This had been a problematic process for the ATP project foundries. The main issue was similar to that limiting the quality of the polysilicon anchor fill, keyhole formation during the fill of the SCS structures with TEOS (tetraethylorthosilicate). In addition to filling up the 6 um deep SCS structures, enough TEOS had to be deposited to allow chemical mechanical polishing of the TEOS to planarize the surface and leave approximately 2 um on the surface as a planar sacrificial layer.

PECVD (Plasma Enhanced Chemical Vapor Deposition) TEOS had been chosen because of it can provide better and thicker conformal coatings than other oxide processes (e.g., PECVD silane, LPCVD silane, and LPCVD TEOS). Work by the ATP foundries had failed to produce a keyhole free TEOS fill (Fig. 15). These keyholes can open up during CMP. The chief effect of this poor planarization is the formation of undesirable polysilicon "stringers" which are formed on the bottom of polysilicon structures when the polysilicon is deposited on the TEOS and into the keyholes (Fig. 16). Even if the keyholes do not open, poor planarity can lead to trapped CMP slurry (Fig. 17).

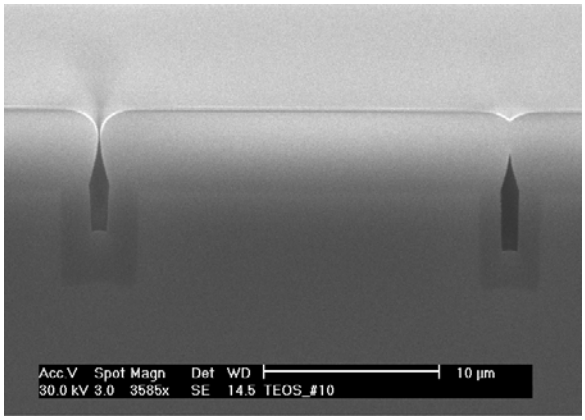


Figure 15. Keyholes in ATP TEOS fill

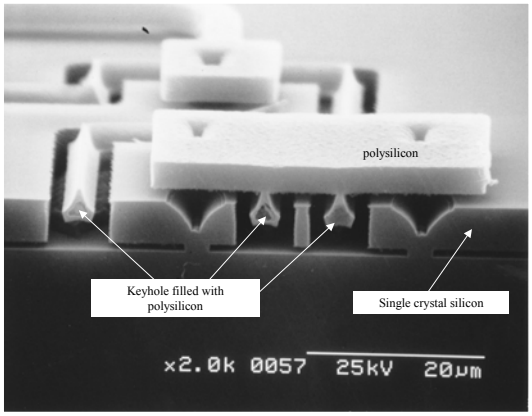


Figure 16. Polysilicon "stringers" on ATP parts

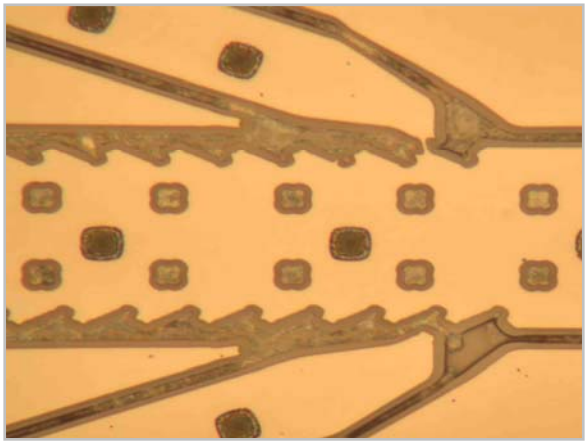


Figure 17. CMP slurry trapped in poorly planarized TEOS.

Several recommendations had been made by the ATP team for improving the TEOS fill, from using a specific too vendor that claimed better conformality to using boron and/or phosphorus-doped oxide (BPSG and PSG) which could be reflowed to refill the holes. Although the TEOS deposition and CMP occur late in the process (about halfway through), ITC staff started work on TEOS deposition and CMP early in the process development cycle. They took advantage of the tool installation and qualification to work with the vendor of the STS PECVD tool to develop a deposition and etch process for TEOS. The process was first developed with silane based oxide (less conformal) at STS under subcontract with Infotonics. Fig. 18 is a cross section of some trenches with a 1:1 (height to width) aspect ratio that have been filled with a silane deposition / etch process. This work demonstrated that the keyhole buried in the oxide could be eliminated by depositing oxide, then etching it back, and redepositing. The etch-back preferentially attacks the oxide at the corners of the vias where the oxide buildup usually occurs that pinches the via off.

The Foundation Process requirement, however, was to fill a 1.25:1 or higher aspect ratio trench. This development work was performed at Infotonics using TEOS, again because of its better conformal coverage of the sidewalls and an etchback process (Fig. 19.)

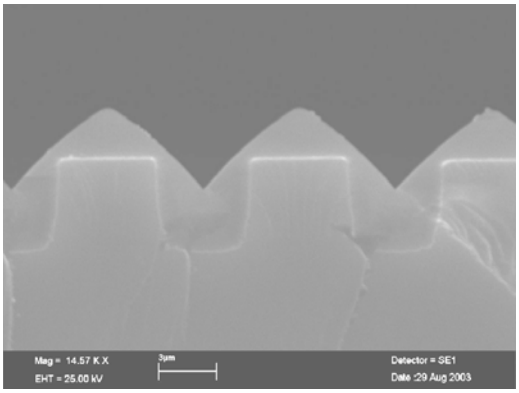


Figure 18. Silane based oxide trench fill using deposition/ etch process.

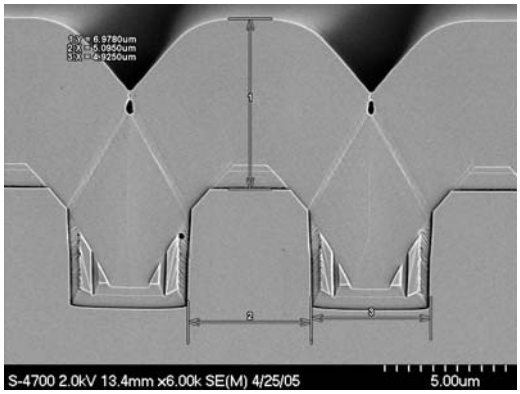


Figure 19. Keyhole free TEOS based trench fill. Artifacts are due to BOE decoration to delineate oxide from silicon in the SEM.

2.5. CMP Oxide Planarization

In order to provide the planar surface upon which to complete the Foundation Process surface micromachining processes, a chemical mechanical polishing process had to be developed. In the context of the ATP process, which is a multi-user process, the CMP process had to satisfy several different device types. The polishing process can be made very selective to silicon nitride, but not so much to silicon. If as planned, nitride is used as the "etch stop", it is necessary to remove all of the overlying oxide with CMP. If it is not removed, then when hot phosphoric acid is used to strip the nitride, the areas where nitride is covered with oxide will not be removed, since hot phosphoric is very selective to oxide. This can leave areas of silicon that are intended to be electrically accessible covered with an insulating layer of nitride. If the CMP is continued to the point where the oxide is all removed, a risk remains that the nitride will be polished through in other areas, and perhaps into the underlying silicon. This can lead to damage to structures such as silicon waveguides. Initially, we used a slurry that was not sufficiently selective to nitride and suffered from some of these issues. This particularly was an issue in Year 2 when we were fabricating the Reconfigurable Optical Add-Drop Multiplexer and optical waveguides. The wafers, which contained both optical devices as well as MEMS devices (they were multi-user wafers), were split so that only optical devices yielded on some wafers, while other devices yielded on other wafers. In this way we could tune the CMP to the devices desired. Figs. 20 and 21 show SEMs of two areas of a wafer polished down to the nitride. Because of the variation in remaining nitride, the oxide will stick up above the Si different heights when the nitride is stripped. Fig. 22 shows a wafer CMP'd down to about 1 um above the nitride. Fig. 23 is a plot of the remaining oxide thickness uniformity across the wafer. The ability to control the final oxide thickness to 3000 A across the wafer indicates that it will be possible to omit the nitride altogether and polish to the desired thickness. This will eliminate the need to deposit and strip the nitride.

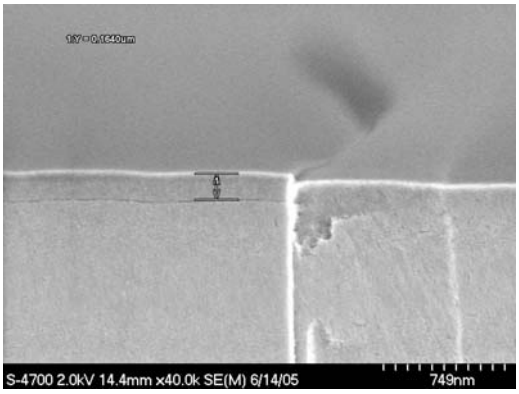


Figure 20. Oxide CMP'd to silicon nitride. 0.08 um of nitride remains

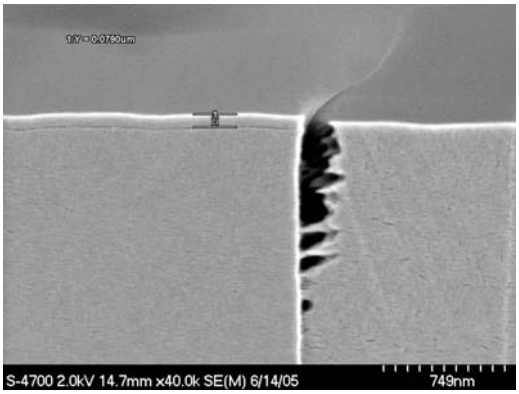


Figure 21. Oxide CMP'd to silicon nitride in another area. 0.16 of nitride remains

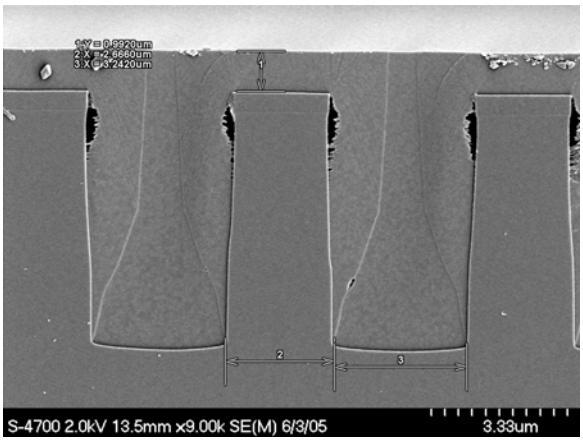


Figure 22. Wafer after trench fill and CMP

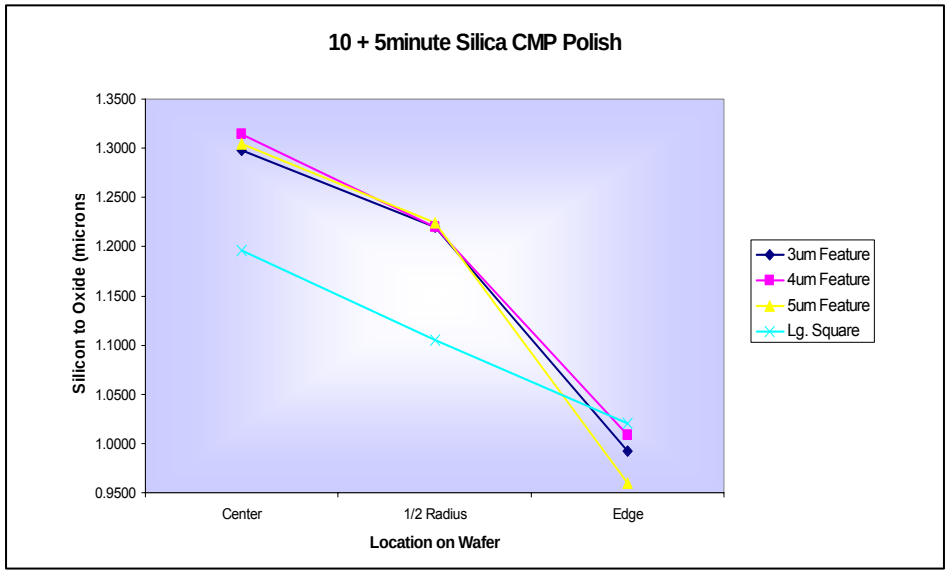


Figure 23. Oxide thickness uniformity across wafer after CMP

2.6 Low stress polysilicon and silicon nitride film development.

The surface micromachining layers of the Foundation Process require the development of a low stress silicon nitride film LPCVD (Low Pressure Chemical Vapor Deposition) process for mechanical structures such as membranes and electrical isolation and a low stress polysilicon film LPCVD process for the surface micromachined mechanical structures such as hinges, resonant beams, cantilevers, comb drives, etc. Development of each of these types of films required a design of experiments (DOE) approach. The DOE for the polysilicon process development is outlined below.

The goals of the polysilicon process DOE were to minimize refractive index variation, maximize deposition rate, minimize thickness variation, and control stress < 250 MPa. The factors varied in the DOE were:

SiH4 flow: 120 – 400 sccm (silane is the precursor gas which is decomposed in the furnace to produce silicon)
Pressure: 180 – 400 mTorr
Temperature: 550C – 600C

The output responses measured were:

Thickness & Uniformity
Refractive Index & Uniformity
Deposition Rate & Range
Stress
Particle count

The DOE used a Box-Behnken Design in which pairs of the inputs are varied at their high and low limits while the third is held at its centerpoint. The design is shown in Table 4, where + and – represent the high and low values of each input range, and 0 represents the centerpoint. 15 runs are required.

Run	SiH4 flow	Pressure	Temperature
1	-	-	0
2	-	+	0
3	+	-	0
4	+	+	0
5	-	0	-
6	-	0	+
7	+	0	-
8	+	0	+
9	0	-	-
10	0	-	+
11	0	+	-
12	0	+	+
13	0	0	0
14	0	0	0
15	0	0	0

Table 4. Box-Behnken DOE

The data generated by the DOE are shown in Fig. 24. Each of the responses is plotted against the inputs to locate the desired process parameters. The optimized process outputs are listed in Table 5. The data are then confirmed by monitoring the process with SPC charts as shown in Fig. 25.

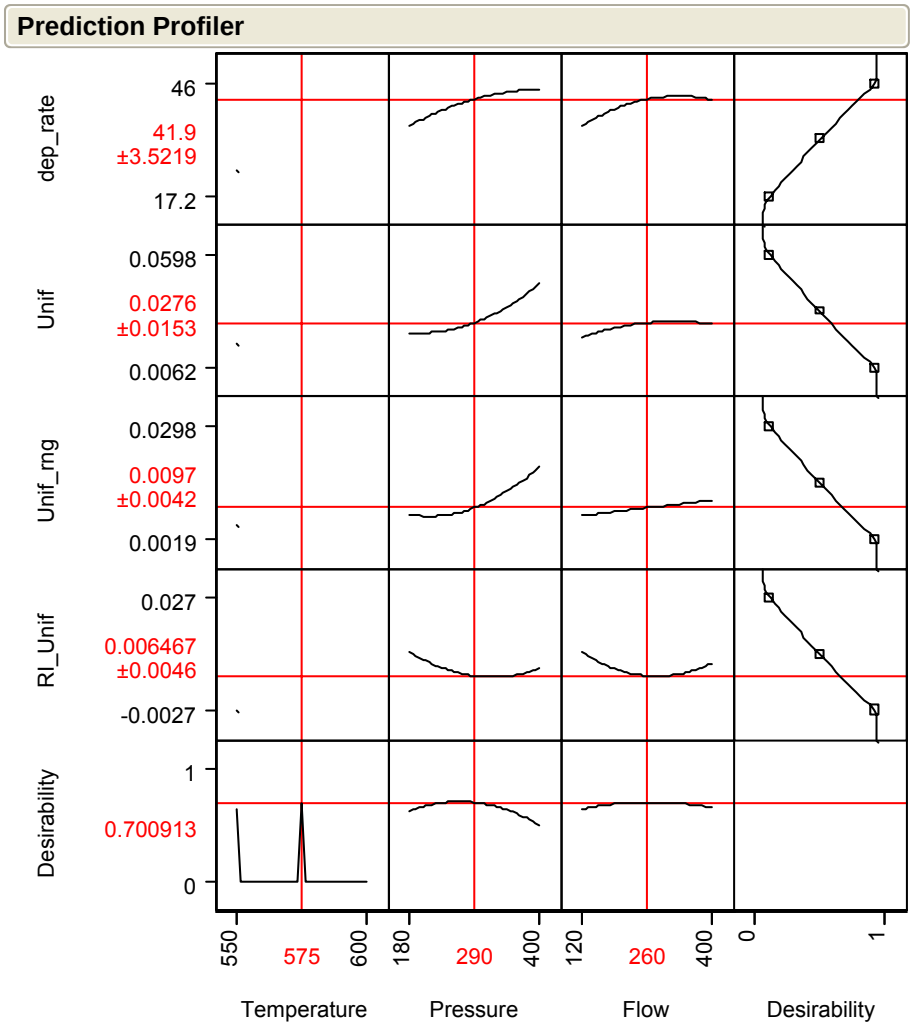


Figure 24. **LPCVD polysilicon DOE results**

	Nominal	Range
Deposition Rate	1.00	1.00
WIW Uniformity	0.97	0.99
Refractive Index	0.72	0.80
R.I. WIW Uniformity	0.99	0.78
Stress	0.75	0.78
Particle	0.78	NA

Table 5. Optimized LPCVD polysilicon physical parameters.

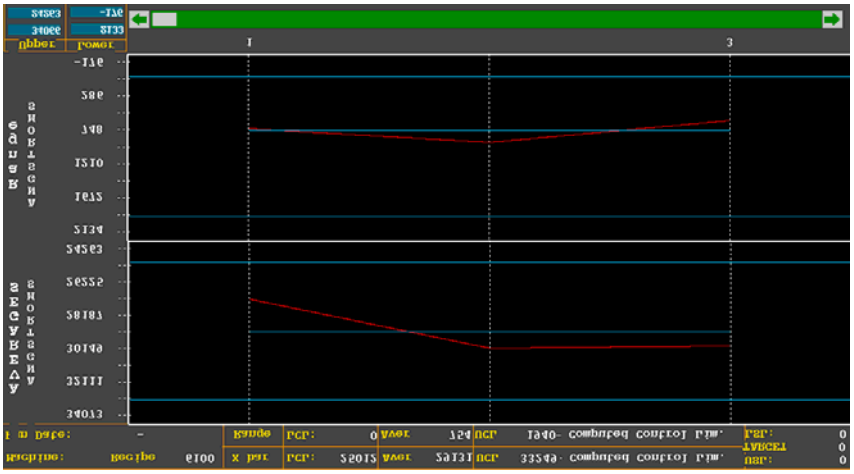


Figure 25(a) Thickness

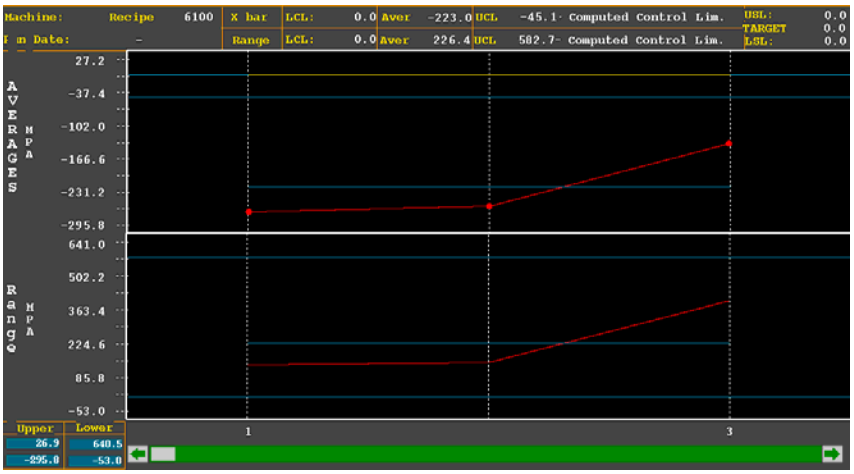


Figure 25(b) Stress

Figure 25(c) Refractive Index

Figure 25. **SPC Charts for (a) Thickness, (b) Stress, and (c) Refractive Index**

3. Applications of the Foundation Process: Waveguides and the Reconfigurable Optical Add/Drop Multiplexer (ROADM)

The Foundation processes were applied in Year 2 to the development of a Reconfigurable Optical Add/Drop Multiplexer (ROADM), including the development of a smooth waveguide fabrication process.

3.1. R-OADM Design and Layout

On-chip integration of optical switching and planar light circuits has the potential to greatly reduce the size and manufacturing costs of multi-component optical equipment such as Reconfigurable Optical Add/Drop Multiplexers (ROADMs). Infotonics Technology Center has developed a platform for integrating MEMS optical waveguide switches with Planar Light Circuits (PLCs) using a silicon on insulator (SOI) platform, which provides capability for monolithically integrating optical, mechanical and electrical functions. The use of a silicon platform enables fabrication of our components using the vast infrastructure and process development available for semiconductor IC manufacturing at silicon foundries. Since the MEMS switches and waveguides are fabricated in the same material, single crystal silicon, there are no stress and strain issues as exist with heterogeneous materials sets such as silica-on-silicon.

A schematic diagram of a R-OADM is shown in Figure 26. The functions of a R-OADM include demultiplexing the input signal into individual wavelengths, dropping the selected wavelengths, adding selective wavelengths, and recombining (multiplexing) the signals back into the output channel.

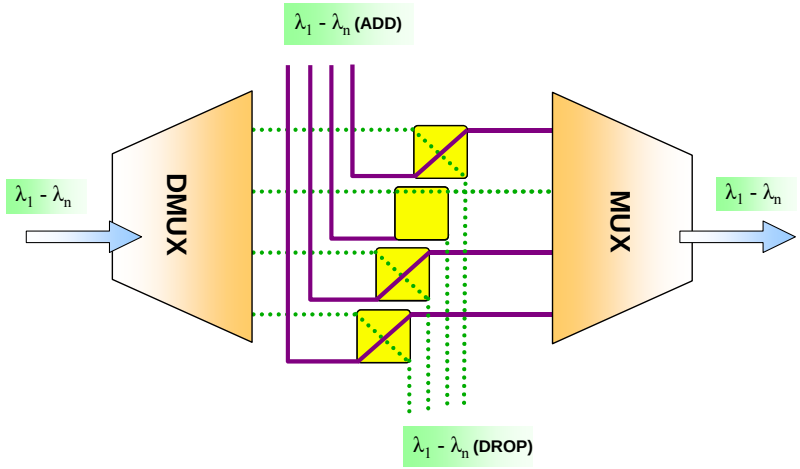


Figure 26. **Reconfigurable Optical Add/Drop Multiplexer (R-OADM)**

The chip layout of the R-OADM device is shown in Figure 27. Two Arrayed Waveguide Gratings (AWG) were designated as a demultiplexer and a multiplexer. There are 8 “add” channels and 8 “drop” channels for 8 different wavelengths to be added into or dropped out of the device. Straight waveguides are designed for characterizing the optical performance such as insertion loss, coupling efficiency, etc. The sidewall roughness of waveguides is measured from these straight waveguides. There are many mechanical and electrical test structures on the chip as well. These test sites provide various material properties and information for diagnosis purposes.

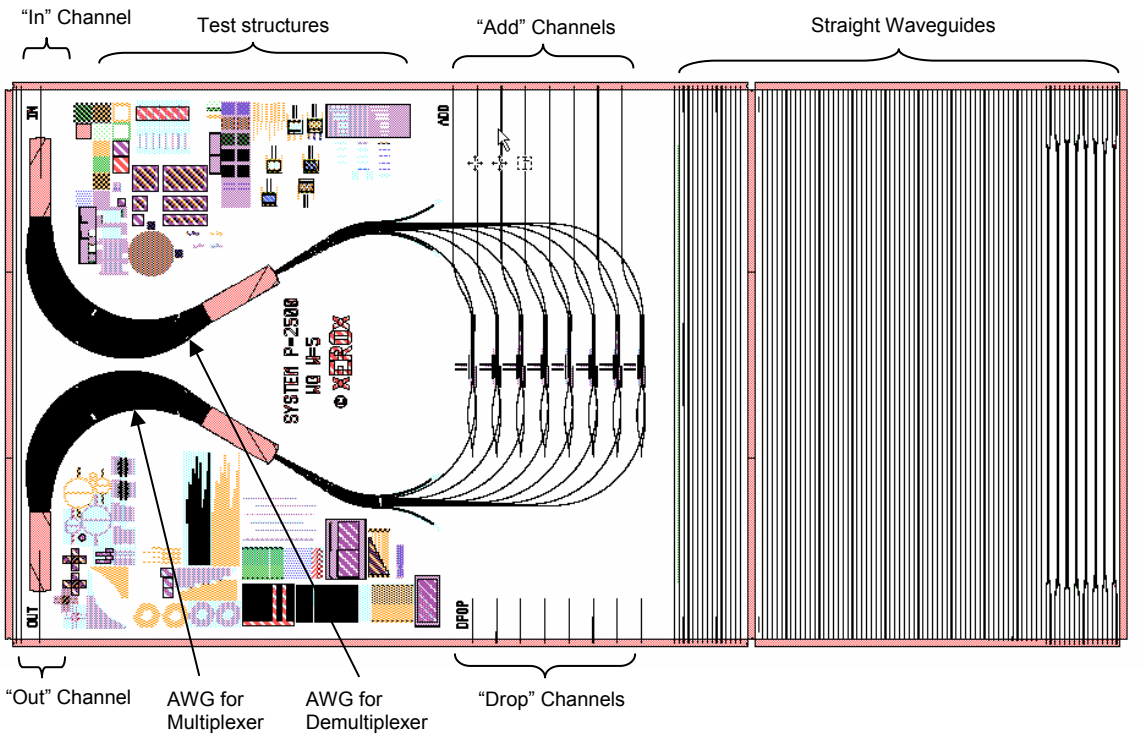


Figure 27. Chip layout for R-OADM. The size of this chip is 15 mm by 30 mm. The typical waveguide width is 5 µm.

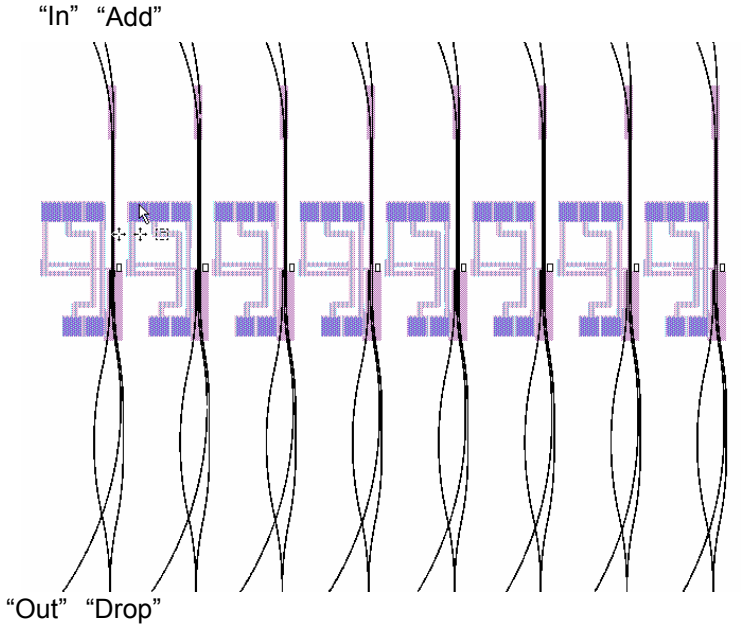


Figure 28. Eight waveguide switches on the R-OADM device. The blue pads are the metal contact bond pads for electrical contact.

Waveguide switches are part of the R-OADM for selecting specific input signals between “In” and “Add”, and selecting the output signals between “Out” and “Drop”. Figure 28 shows the 8 waveguide (WG) switches that were included in the chip. The chip is capable of performing 8x8 optical switching. Figure 29 shows an enlarged layout drawing for WG switches. The WG switch is driven using a heat actuator. The latching is provided by a latching mechanism with 2 heat actuators. The switches are latched so that no power is required except when changing the state of the switches, allowing the switch states to retain their configuration if power is lost. This is an essential feature for safety and energy saving. Figures 30-35 are SEM (scanning electron microscope) details of the ROADM chip.

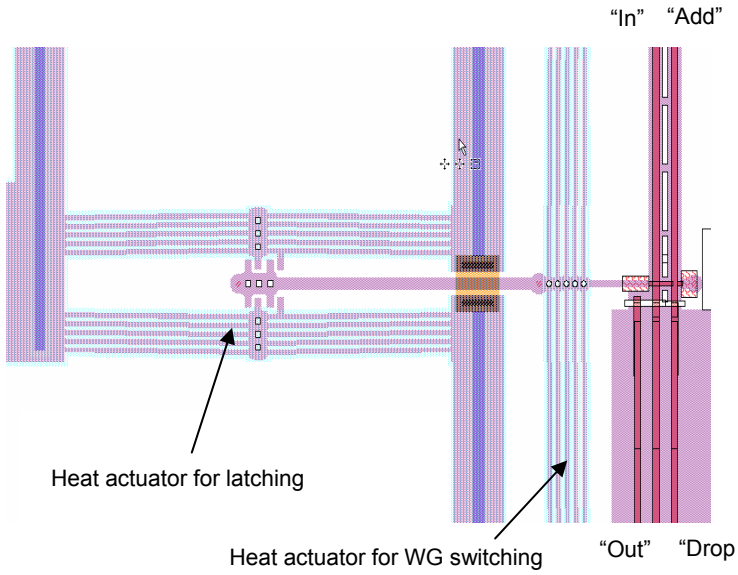


Figure 29. The optical switches consist of 3 heat actuators and a latching mechanism

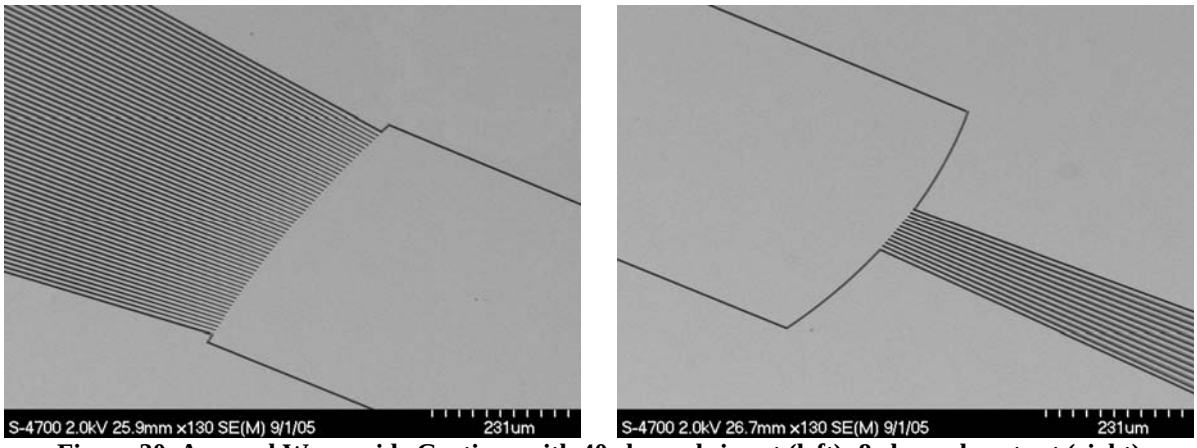


Figure 30. Arrayed Waveguide Gratings with 40 channels input (left); 8 channels output (right)

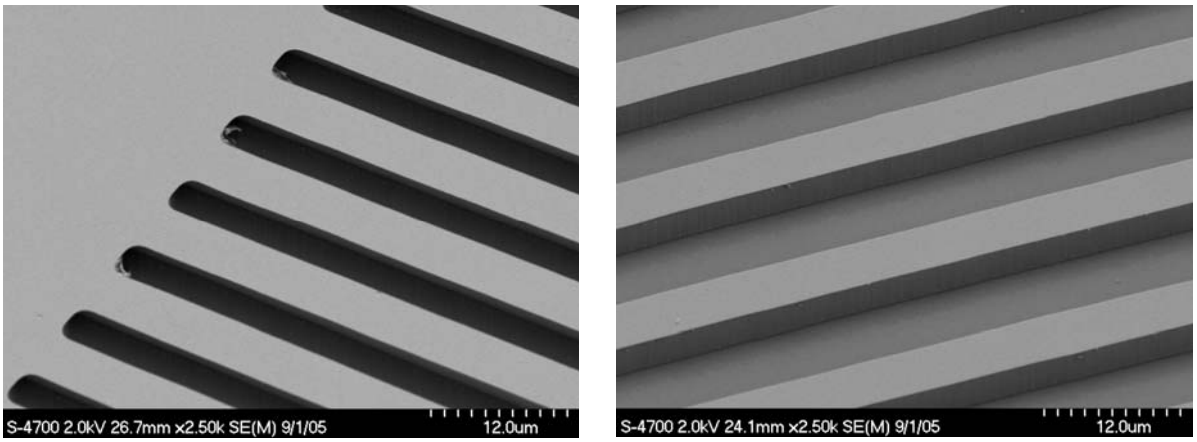


Figure 31. The output areas of AWG (left); the straight waveguides (right)

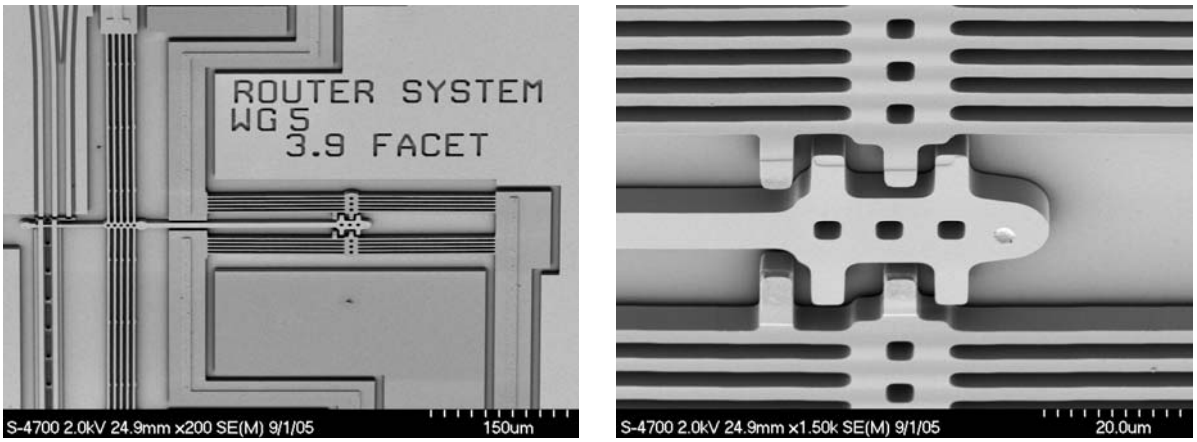


Figure 32. The actuators for optical switches (left); the latching mechanism (right)

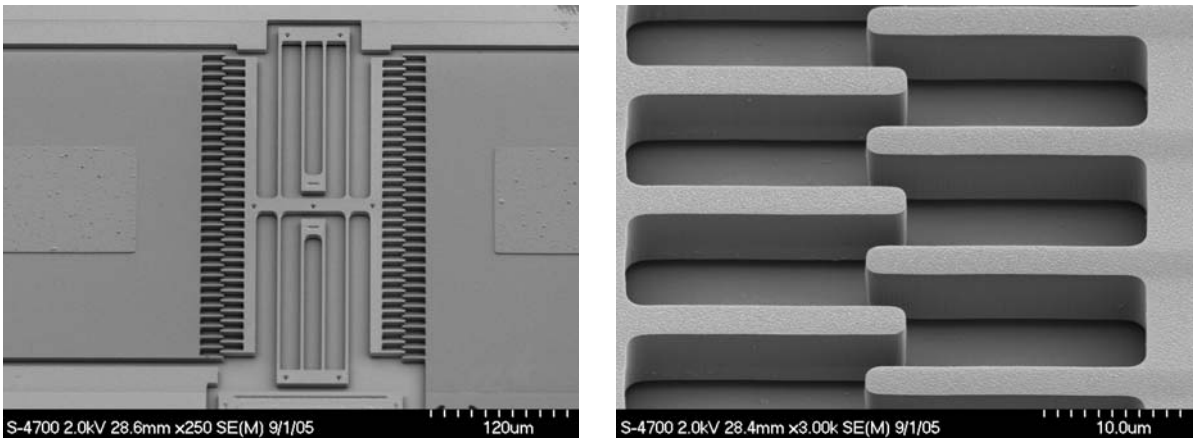


Figure 33. Resonator as a test structure to study the mechanical properties (left); the comb-drive teeth structure (right)

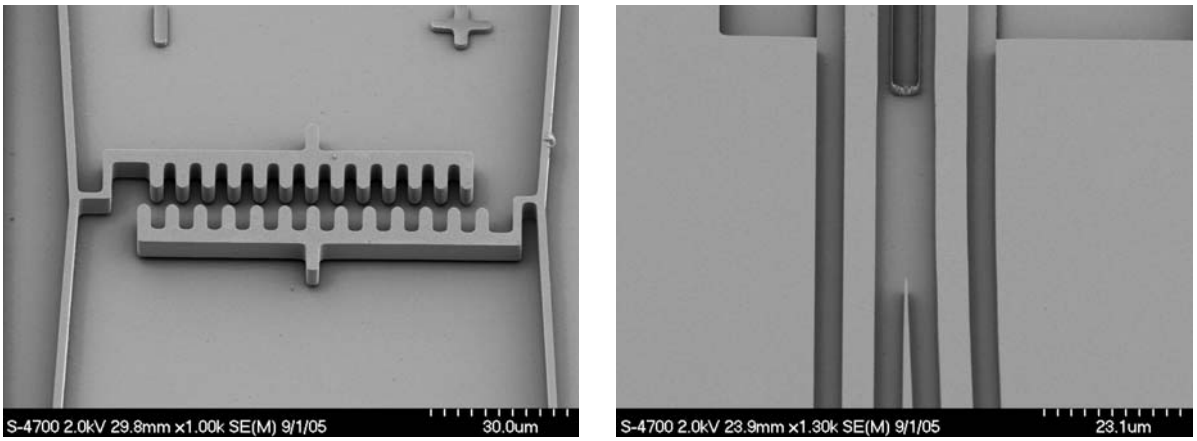


Figure 34. The strain gage to detect the residual stress (left); two waveguides merged in the output area.

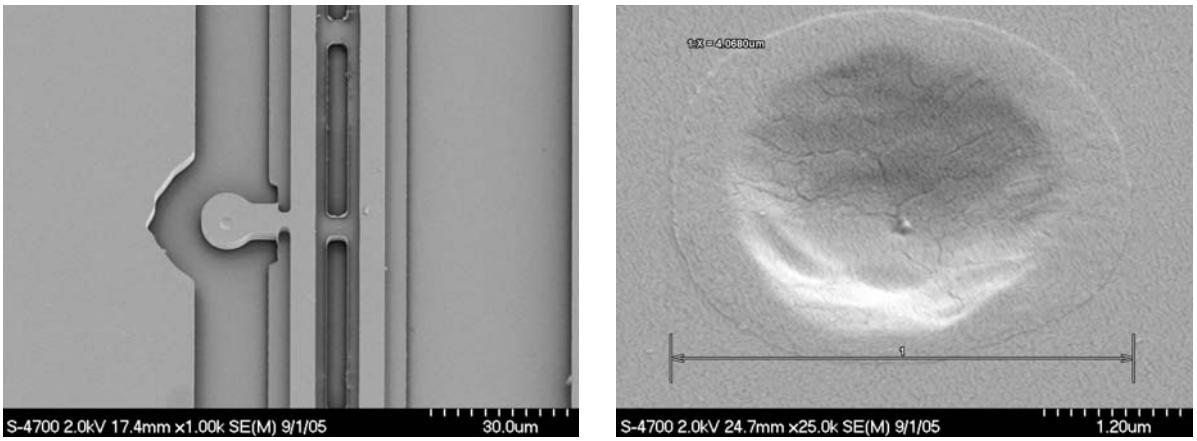


Figure 35. Waveguide switches with a side dimple to prevent stiction (left); the completely-filled dimple without any void (right).

3.2. Microfabrication Process Sequence

The device wafers are SOI (silicon-on-insulator) wafers that consist of a 5-μm thick single crystal silicon (SCS) layer on top of a 1-μm buried silicon dioxide (BOX) layer. Figure 36 shows the schematic cross-section view of this process (9 masks). (Hard masks for etching and etch stops have been left out for clarity.) The SCS layer is etched 0.3 μm deep using the first mask (named SCS Shallow Etch, Figure 36A). This etch is used to pattern structures such as alignment marks and optical gratings. The second mask (SCS Doping, Figure 36B) is for selective phosphorus doping in the desired areas on the SCS layer. Unlike blanket doping, this process avoids optical losses due to the high doping levels in the optical path of waveguides.

The third mask (SCS Anchor, Figure 36C) and fourth mask (SCS Dimple, Figure 36D) can be patterned using DRIE (deep reactive ion etching). The anchor etch is completely through the BOX to provide mechanical connection to the handle wafer. The dimples are anti-stiction structures. A layer of polysilicon is deposited to fill the anchor and dimple holes. The anchor mask can be skipped using timed-release in the final release process. However, the anchor structures provide better latitude for the release process. The polysilicon is then blanket-etched away to expose the SCS layer again (Figure 36E).

The next mask (SCS Precision Cut, Figure 36F) is a high precision cut to control structure dimensions, such as waveguide gaps, on the SCS layer. The sixth mask (SCS Medium Etch, Figure 36G) offers an intermediate SCS etch, and does not go all the way through the SCS. It is used to pattern structures such as waveguides and gratings within the SCS layer. The last mask on the SCS layer (SCS Final Cut, Figure 36H) is DRIE through the SCS layer. This is mainly to etch away large areas in SCS to create electrical devices such as heat actuators, while the previous SCS Precision Cut only etches trenches or holes in very small and similar dimensions to avoid loading effects.

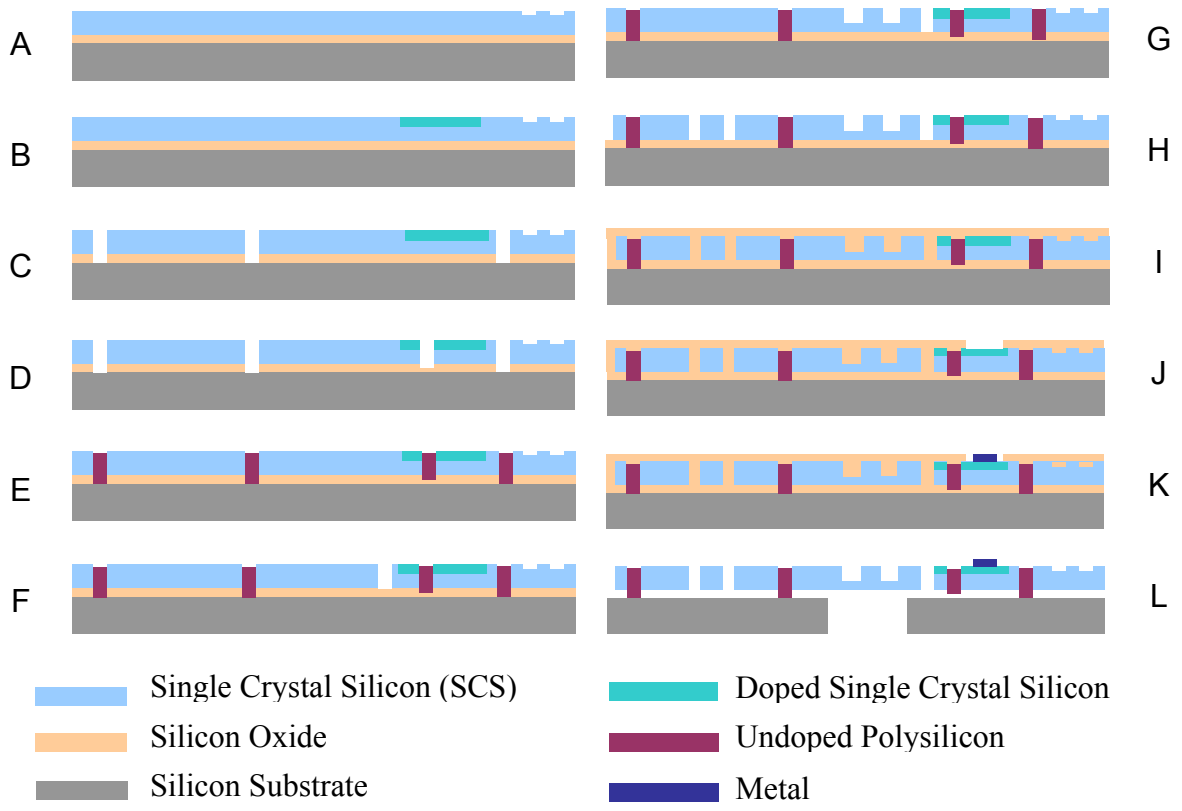


Figure 36. Step-by-step cross-section view of the microfabrication process. There are totally 9 masks in this process.

One of the key challenges for MEMS fabrication is to overcome the topography created by DRIE. After large areas of the SCS layer are etched away, it is very difficult to use thin photoresist for photolithography. Thus, it is necessary to level the topography. The next step is to fill the etched SCS areas with silicon dioxide using plasma enhanced chemical vapor deposition (PECVD). An 8-μm conformal PECVD TEOS (tetra ethyl ortho silicate) oxide deposition/etch gap-fill process has been developed for this step without buried key holes. The thick oxide layer is then planarized using chemical mechanical polishing (CMP), which uses a silicon nitride layer under the TEOS as a polishing stop. The nitride layer is removed after CMP using hot phosphoric acid (180°C for 30 min).

Mask #8 (TEOS Etch, Figure 36J) is used to open areas in the TEOS layer for metal contact. Metal such as Cr/Au is deposited using lift-off techniques with mask #9 (Metal, Figure 36K). After metal deposition, the structures can then be released using a wet process (HF solution) or a dry process (HF vapor) (Figure 36L). In many designs, Masks #8 can be eliminated to shorten the process.

Six of the 9 masks are for the patterning of the SCS layer including three different etching depths in SCS layer (0.3 μm, 3 μm, and 5 μm). The various etching steps enable designs such as optical gratings, channels, waveguides, and actuators. Other advantages for these SCS processes include: (1) precise dimensional control (within ±0.2 μm error for optical devices), (2) dimples on released SCS structures (preventing stiction), and (3) anchoring of the SCS layer (for long release in HF). The mask for confining doping areas (mask #2) avoids the large loss of optical signals in waveguides of the doped SCS areas.

3.3. Microfabrication Process Development

3.3.1 Chemical Mechanical Polishing (CMP)

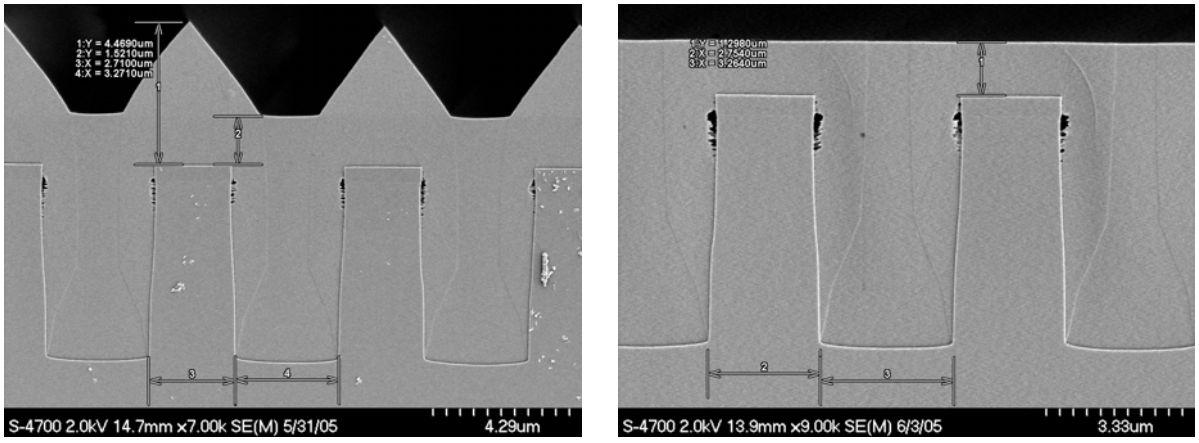


Figure 37. Wafers with 5 μm deep trenches covered with 8 μm TEOS oxide (left); Wafers after CMP with about 1.3 μm TEOS oxide still on the surface

The objective of CMP is to planarize the wafers that have 5 μm deep trenches created by etching of actuators and waveguides. The first step is to deposit PECVD silicon oxide. The wafer profile after the oxide deposition was shown in Figure 37 (left). There are two methods for CMP. The first method is to time the CMP so that there is about 1 μm oxide left on the surface, as shown in Figure 37 (right). The advantage of this method is no additional stop layer is needed and the process is simpler.

The second method is to CMP all the way to eliminate all TEOS oxide until a stop layer is reached. The stop layer (silicon nitride in this study) should shows high selectivity in CMP rate. Figure 38 shows that both small and large trenches are still filled with TEOS oxide, while the oxide on the upper surface has been removed completely by CMP. Both methods have been tried in the process development.

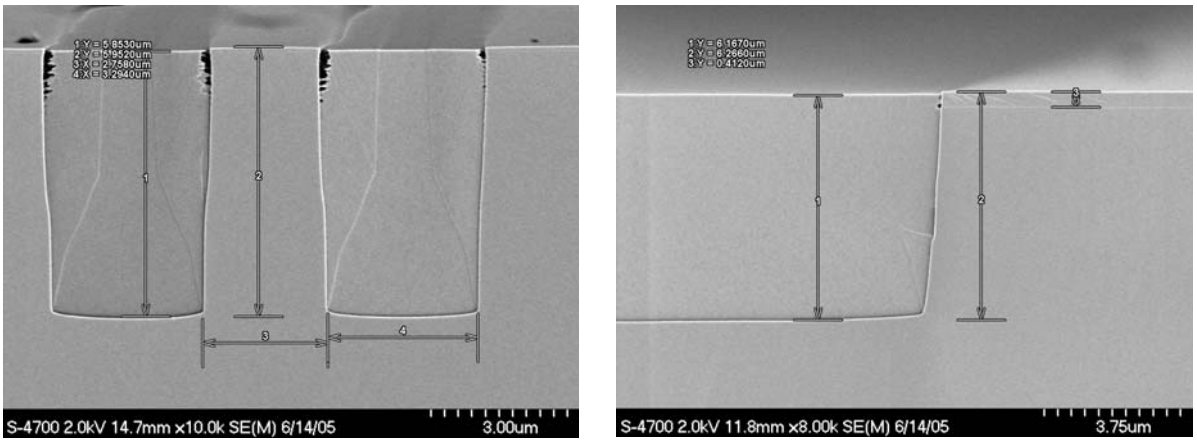


Figure 38. Small trenches after CMP stop on silicon (left); large trench after CMP (right)

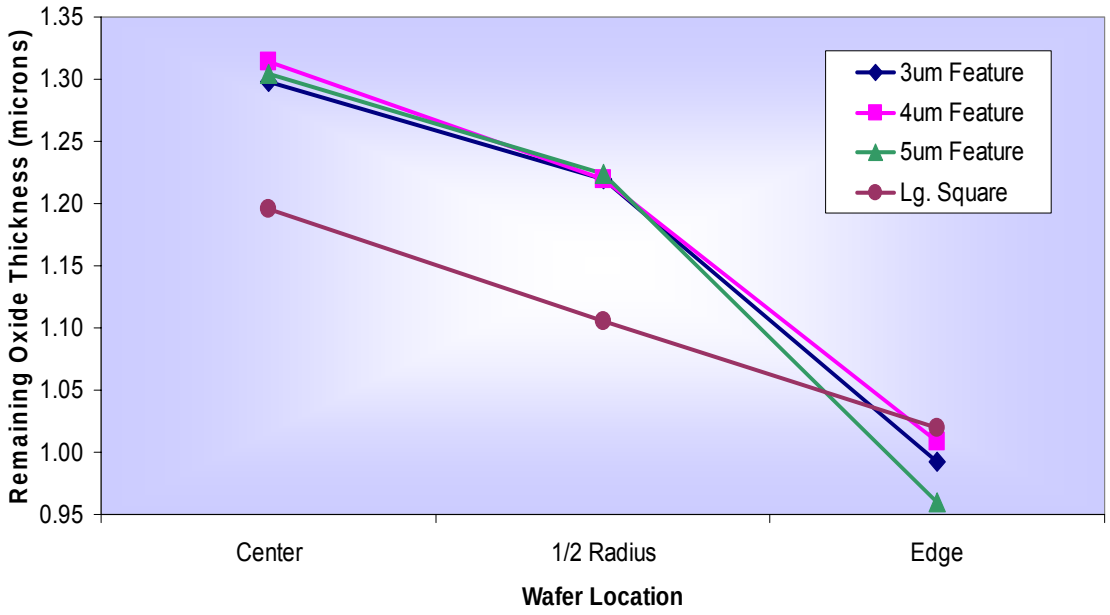


Figure 39. WIWNU measurement for wafers after timed-CMP

To characterize the CMP results, the remaining oxide thickness were measured across the wafer. Within-wafer-nonuniformity (WIWNU) was measured as the standard deviation of 49-point oxide thickness measurement. Dishing is measured as the oxide surface dip in the center of the trench since slurry tends to remove more oxide in the trench center than at the edge. Both parameters are import to produce optical quality flat surface for optical applications.

The results showed that timed-CMP is uniform from center to edge. The remaining oxide thickness is 1.30 μm at center, 1.20 μm at ½ radius, and 0.99 μm at edge (Figure 39, blue line). The maximum difference in remaining oxide thickness is about 0.3 microns. All different sizes of trenches (3 μm to 5 μm) showed consistent polish rates (Figure 39). The large features showed only minimum dishing at about 0.3 microns. That is, the center of the large trench only has about 0.3 microns lower surface than the edge. This demonstrates that CMP can produce a very flat surface after 6 μm of topography.

3.3.2. Dry Etching for Reduced Sidewall Roughness

Two silicon dry etching tools were investigated. One is LAM 9400 (manufactured by LAM Research) and the other is STS ASE (manufactured by Surface Technology Systems). Both machines use reactive ion as the etchants, while ASE has ICP (Inductively Coupled Plasma) for higher power plasma. The variables in the experimental design are etchant gas type (such as Cl_2, HBr, or SF_6), etching gas flow rate, gas ratio, plasma power, and chuck temperature. The etching time is set to etch the required 3 microns depth in the single crystal silicon. The surface profile and the sidewall surface roughness were studies. Table 6 shows the recipe in the etching matrix on both machines. All the wafers used photoresist as the mask in the etching.

LAM Recipes

	Gas Flow (sccm)						Power (Watts)		Chuck	
Wafer #	**CL_2**	**HBr**	**SF_6**	**CHF_3**	**He**	**O_2**	**Upper**	**Lower**	**Temp (^oC)**	**Time (mm:ss)**
1184-06	30	120	---	---	---	---	350	70	60	17:00
1184-03	---	---	23	---	170	20	500	25	20	4:00
1184-02	---	---	23	---	170	20	500	25	20	1:00
1200-04	---	---	23	---	170	---	500	25	20	1:00
1184-05	---	---	23	---	170	20	500	25	60	1:00
1184-19	---	---	23	---	170	25	500	25	20	1:00
1184-18	100	100	---	---	---	---	800	60	40	1:00
1184-04	100	100	---	---	---	---	800	60	40	6:00
1200-15	200	200	15	40	---	---	800	62	40	5:00

ASE Recipes

	Gas Flow (sccm)						Power (Watts)		Chuck	
Wafer #	**C_4F_8**	**SF_6**	---	---	---	---	**Upper**	**Lower**	**Temp (^oC)**	**Time (mm:ss)**
1184-07	90	40	---	---	---	---	800	15	20	11:30
1184-01	90	40	---	---	---	---	800	15	20	12:45
1184-20	65	45	---	---	---	---	600	12	20	12:45

Table 6. The design of experiment for dry etching

The results showed quite a range of etching profiles as expected (Figure 40). The etchant type was found to be the main factor for the etching profile. This was mainly due to the etching isotropy and mask erosion from the etching. The desired waveguide profile is shown on the left of Figure 40. It was found that Cl_2/HBr based etching (Figure 40, center) tends to etch the photoresist mask more than SF_6 based etching.

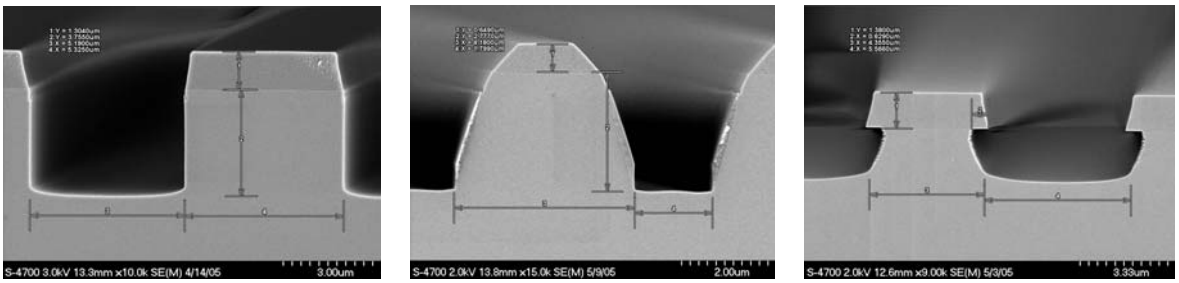


Figure 40. Examples of etched waveguide profile from the design of experiment (DOE): wafer # 1184-02 (left); wafer # 1184-04 (center); wafer # 1200-04 (right)

SEM (scanning electronic microscopy) pictures were primarily used to select the process conditions for further study. Among the design matrix, three samples showed relatively straight and smooth sidewall (1184-02, 1184-07, and 1184-20). These conditions plus 1200-15 (as a typical reference) were chosen for etching waveguides on SOI wafers.

3.3.3. The Measurement of Sidewall Roughness

There were 3 techniques used for measuring sidewall roughness: surface profilometry, atomic force microscopy (AFM), and 3D image analysis with SEM. As indicated previously, four dry etching conditions were selected. There were one SOI wafer (for devices) and one test wafer for each etching condition. Table 7 shows the design of experiment for SOI wafers. Only one mask (the waveguide mask) was used for this test. The same hard mask (4000Å of PECVD silicon oxide and 5000Å PECVD silicon nitride) in the R-OADM process was used for this study. After 3-μm etching in silicon, the hard mask was removed using hot phosphoric acid (at 180°) and buffered oxide etch (BOE, 6:1 ratio).
Surface profilometry was carried out using a surface profilometer (Alpha-Step IQ made by Tencor). The tip size is 300 nm. The advantage of this technique is to allow a long scanning length (such as the sidewall of a straight waveguide). The scanning distance can be over 2000 μm in some cases. This would provide more representative roughness data. The disadvantages are the relatively large tip size compared to the roughness range in the sample. The typical roughness after dry etching is around 0.1 to 0.3 μm from top to bottom. The tip size needs to be at least 5x smaller than that range. The surface profilometer also needs to be on a vibration-free environment for accurate reading. Figure 41 shows the sample preparation for AFM and SEM. Similarly, chip samples for surface profilometer also need to stand up by the side for scanning.

SOI Wafer	Test Wafer	Etch Tool	Gas Flow Rate (sccm)	Power (Watts) Upper/Lower	Comments
6021-01	1184-12	ASE	C_4F_8 = 90; SF_6 = 40	800W/15W	= 1184-07
6021-02	1184-11	LAM 9400	SF_6 = 23; He = 170;O_2 = 20	500W/25W	= 1184-02
6021-03	1184-10	LAM 9400	Cl_2 = 200; HBr = 200; SF_6 = 15; CHF_3 = 40	800W/62W	= 1200-15
6021-04	1184-09	ASE	C_4F_8 = 65; SF_6 = 45.	600W/12W	= 1184-20

Table 7. Design of experiment for waveguide sidewall roughness. The details of the process conditions are also shown in Table 6.

Figure 41. Chip sample set-up for AFM (left); SEM (right)

Wafer	Sample #	Ra (nm)	Ave. Ra (nm)	Rq (nm)	Ave. Rq (nm)
1184-10	1	30.8	31.2	40.7	41.6
	2	36.7		49.1	
	3	26		35	
1184-11	1	19	28.6	23.9	36.8
	2	24.8		32.5	
	3	42.1		54	
1184-12	1	45.5	33.1	60.3	43.8
	2	19		25.5	
	3	34.8		45.5	

Table 8. The roughness measurement from the surface profilometer (Alpha-Step by Tencor)

The results of roughness measured by surface profilometer are shown in Table 8. The roughness is presented by the average roughness, Ra, and the root-mean-square average roughness, Rq. For calculating Ra, a mean line is first found that is parallel to the general surface direction and divides the surface in such a way that the sum of the areas formed above the line is equal to the sum of the areas formed below the line. The surface roughness Ra is now given by the sum of the absolute values of all the areas above and below the mean line divided by the sampling length. For Rq, it is calculated by the root-mean-square of the areas over the scanned length. The value of Rq is typically larger than Ra. For a perfect sine wave roughness, the value of Rq is 1.11 larger than the value of Ra.

Table 8 shows the roughness measured from surface profile. The average roughness is on the order of 30 nm. The wafer 1184-11 shows the least roughness among all samples.

AFM (atomic force microscopy) has been known for its superb capability to measure surface roughness. The tip size is small and the accuracy is higher than surface profilometer. However, the sample set-up for measuring the roughness on a 3-μm vertical sidewall is a challenge. In addition, the sampling area is usually very small (about 2 μm x 2 μm). Small localized defects may skew the data. It would not be efficient from a time standpoint to scan a larger area. Besides, the area scanned cannot be easily determined since the cantilever supporting the tip blocks the view from the camera.

Table 9 shows the results from AFM. Since the set-up prevented direct view of the scanned area, it is very difficult to know whether the tip was measuring the desired area. We are trying to install a new camera on an angle so that the tip can be seen during the scanning. Among the test samples, the roughness of 1184-11 and 1184-12 seem to be better than that of 1184-10 (Table 9).

Wafer	Sample #	Ra (nm)	Ave. Ra (nm)	RMS (nm)	Ave. Rq (nm)
1184-10	1	27.88	15.6	38.27	20.8
	2	10.32		13.07	
	3	8.587		11.02	
1184-11	1	3.12	2.7	4.11	3.8
	2	2.49		3.31	
	3	1.32		1.79	
	4	1.41		2.08	
	5	5.13		7.52	
1184-12	1	2.71	2.5	4.35	3.4
	2	3.46		4.17	
	3	1.25		1.59	

Table 9. The roughness measurement from AFM

Recently software has been available to construct a 3D image from a 2D SEM pictures. MeX software (by Alicona Imaging) allows a 3D SEM image calculated from stereoscopic images that are obtained by simple tilting of the stage when SEM pictures are taken. Once the 3D image is generated, the surface profile and roughness can be easily calculated. The advantage of this technique is no additional hardware is needed since SEM pictures have already been collected. However, the roughness in this study is in the nm range which is almost the limit of SEM pictures with good quality. Thus, the 3D image generated was not very sharp and the accuracy of the calculated surface roughness may be low. Nevertheless, the tool may still be useful for relative comparison of roughness.

The results of these SEM-based surface roughness measurements are shown in Table 10. The order of roughness in less than 1 nm, indicating the 3D image has been artificially smoothed when it is constructed from the 2D image.

Wafer	Sample #	Ra (nm)	Ave. Ra (nm)	Rq (nm)	Ave. Rq (nm)
1184-10	1	0.359	0.29	0.745	0.57
	2	0.331		0.673	
	3	0.177		0.282	
1184-11	1	0.39	0.39	0.60	0.60
	2	0.39		0.60	
1184-12	1	0.20	0.24	0.36	0.42
	2	0.26		0.42	
	3	0.26		0.49	

Table 10. The surface roughness calculated from the 3D SEM images by using the MeX software

Figures 42 to 45 are SEM pictures taken directly from SOI wafers. By judging the SEM alone, it clearly shows some difference in roughness among the samples.

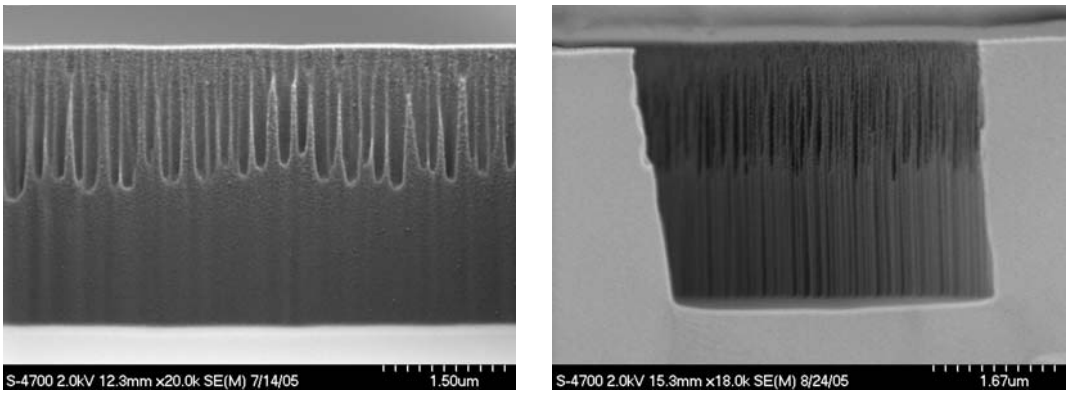


Figure 42. SOI wafer 6021-01, side view (left); waveguide view (right)

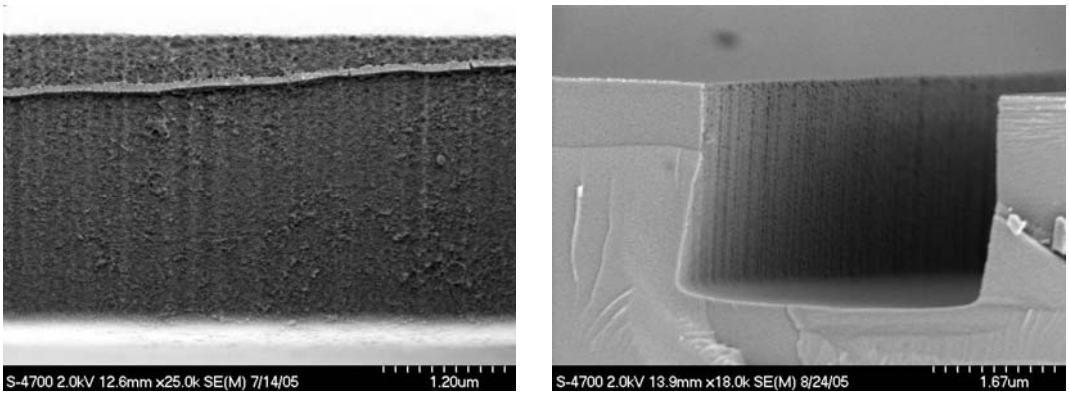


Figure 43. SOI wafer 6021-02, side view (left); waveguide view (right)

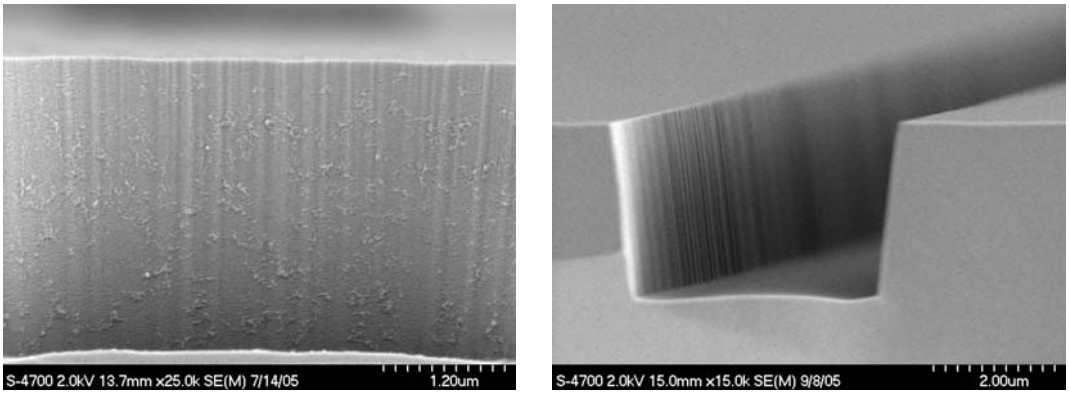


Figure 44. SOI wafer 6021-03, side view (left); waveguide view (right)

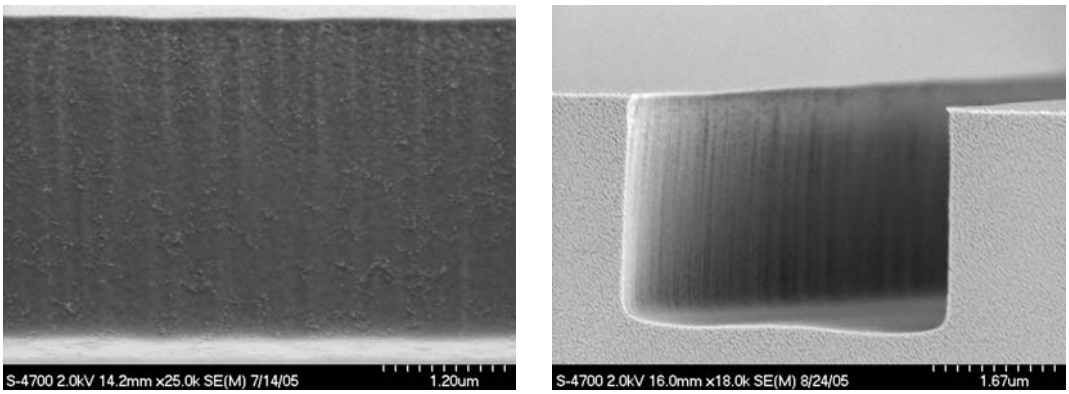


Figure 45. SOI wafer 6021-04, side view (left); waveguide view (right)

Table 11 shows the summary of the roughness measurement. The test wafers (Lot # 1184) were processed at the same time as the SOI wafers (Lot #6021). The test wafers were then sacrificed for roughness measurements with all 3 above-mentioned techniques and the SOI wafers were diced and polished for optical measurement. The optical performance is shown in the following section.

SOI Wafer	Test Wafer	Etch Tool	Process conditions	Type	Ra (nm)	Rq (nm)
6021-01	1184-12	ASE	C4F8, & SF6; 800W/15W; (=1184-07)	Profile	33.1	43.8
				AFM	2.5	3.4
				MEX	0.24	0.42
6021-02	1184-11	LAM 9400	SF6, He, & O2; 500W/25W; (=1184-02)	Profile	28.6	36.8
				AFM	2.7	3.8
				MEX	0.39	0.6
6021-03	1184-10	LAM 9400	Cl2, HBr, & CHF3; 800W/62W; (=1200-15)	Profile	31.2	41.6
				AFM	15.6	20.8
				MEX	0.29	0.57
6021-04	1184-09	ASE	C4F8, & SF6; 600W/12W; (=1184-20)			

Table 11. Summary of all the roughness measurement from all different techniques. The process conditions are detailed in Table 1

4. Optical Performance of Waveguides

4.1 Determination of Anti-Reflection Coating

The waveguide chips from four SOI wafers were diced and polished for optical performance tests. To prevent reflection between the polished waveguide and the optical fiber, a thin layer of anti-reflective (AR) coating was deposited at the end of the waveguides. The materials and the thickness of AR coating were determined to minimize the optical loss.

Figure 46 shows a schematic diagram of the reflection of light with AR coating. Material 1 is air, material 2 is the AR coating, and material 3 is the silicon. The reflective index of material 1 is indicated as n1. To optimize the AR coating, the reflection R1 and R2 should be almost equal. Both R1 and R2 can be expressed by the reflective index of the materials (n1, n2 and n3) as follows.

R1 ~ (n2-n1)/(n2+n1);

R2 ~ (n3-n2)/(n3+n2).

The optimized n2 of AR materials should be around 1.84. Hafnium oxide (HfO_2) has reflective index around 1.97 @ 800 nm. The reflective index would be lower at 1550 nm, which is the wavelength for the waveguide test.

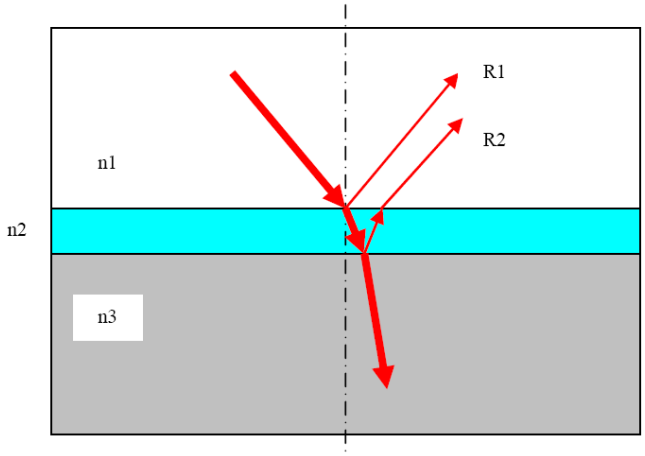


Figure 46. The reflection of light with anti-reflective (AR) coating

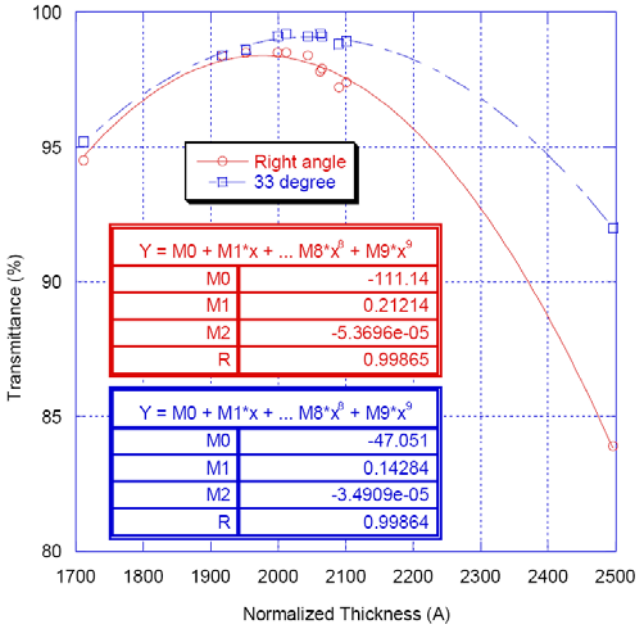


Figure 47. The transmittance of AR coating on silicon wafer as a function of coating thickness

The deposition of HfO_2 was carried out using Leybold APS1104 reactive evaporator system. Advanced Plasma Source (APS), also known as Plasma Ion Assisted Deposition (PIAD), was used to provide a denser film. ESV14 electron beam gun was used for the evaporation. The film thickness was measured using N&K 1700 Metrology System. The optimized thickness of AR coating was determined for maximizing the transmittance. Figure 47 shows the transmittance as a function of hafnium oxide thickness on silicon wafers. The maximum transmittance was determined at 1976 Å for right angle incident or 2046 Å for 33° incident.

4.2 Optical Loss Measurement

The optical loss was measured based on Fabry-Perot transmission fringes through the straight waveguide. The technique relies on the use of the waveguide itself as a Fabry-Perot interferometer. The advantages of this method are fast, nondestructive, and accurate. The limitation on this method is that it only works for monomodal waveguides, which is not a problem in our case.

First, the output power of the light through the waveguide was measured. Figure 48 shows the typical results of the measurement. The maximum and minimum output intensity (defined as T_{max} and T_{min}, respectively) can be easily determined on Figure 23. The constant, C, of the Fabry-Perot fringes is defined as $C = (T_{max} - T_{min})/(T_{max} + T_{min})$. The optical loss can then be derived using the equation (1):

$$\frac{1-\sqrt{1-C^2}}{C} = Re^{\alpha L} \tag{1}$$

where α is the optical loss, L is the length of the waveguide, and R is the reflective coefficient at the interface of waveguide and air. The value of R is known by

$$R = \left(\frac{N_{eff}-1}{N_{eff}+1}\right)^2 \tag{2}$$

where N_{eff} is the effective reflective index of the waveguide.

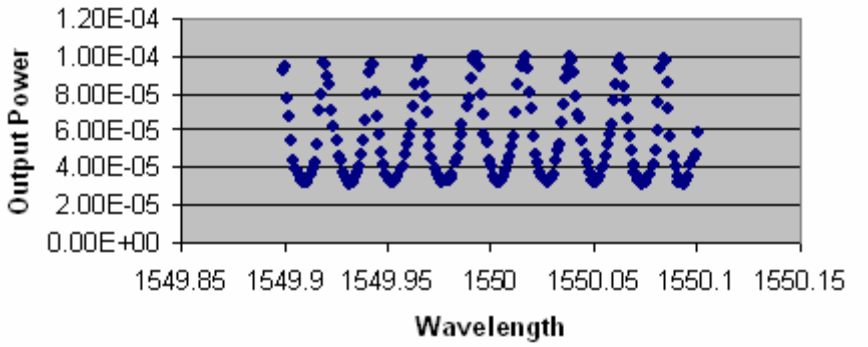


Figure 48. Typical Fabry-Perot fringe pattern on waveguide

The summary of the optical results is shown in Table 12. To compare with a similar waveguide made by a commercial MEMS foundry (Corning IntelliSense), the optical loss of the IntelliSense chip was measured at 1.30 dB/cm. All of the waveguide made here showed better performance than it. This benchmark clearly shows that the capability of microfabrication at Infotonics. Among the 4 SOI wafers, it is found that 6021-03 and 6021-04 has the best optical performance. Although the roughness data cannot be correlated to the optical results, it is clear that the optical results fits very well with the SEM pictures (Figure 49).

The better optical loss than a previously chip could be explained by a couple of factors. First, it is the better lithography tool. Infotonics is equipped with a UltraTech 1x stepper, which offers better resolution (<1 μm) and eliminates number of defects by avoiding contacting wafers. Secondly, the hard mask removal requires the usage of hot phosphoric acid (at 180°C). Although phosphoric acid is known to have very good selectivity between silicon nitride and single crystal silicon, it will probably etch 0.5 to 2 Å/min. That will translate to a total of 15 to 60 Å removal of silicon on the sidewall. If this is the case, it will be very useful for smoothing the sidewall after dry etching. Further tests are needed to confirm this technique.

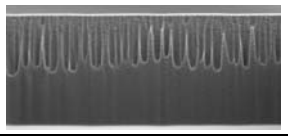
SOI Wafer	Etch Tool	Intrinsic Optical Loss (dB/cm)	Average Loss (dB/cm)	SEM pictures
6021-01	ASE	1.35	1.24	
		1.27		
		1.09		
6021-02	LAM 9400	1.13	1.08	
		0.87		
		1.23		
6021-03	LAM 9400	0.70	0.60	
		0.35		
		0.74		
6021-04	ASE	0.65	0.55	
		0.36		
		0.63		

Figure 49. Summary of optical loss and SEM pictures of waveguides

5. Heat Actuator performance

The R-OADM devices include waveguides and optical switches. The switching function is provided by MEMS heat actuators. The MEMS Motion Analyzer (MMA), made by Umech Technology, was used to characterize the actuation (Figure 50). The MMA takes series of interference image of a moving MEMS device using a strobed light source. By timing these strobed pulses to coincide with specific phases of the motion, the trajectory of the moving MEMS device can be samples and reconstructed. These fringes are used to calculate changes in the height (out-of-plane) motion or lateral (in-plane) motion.

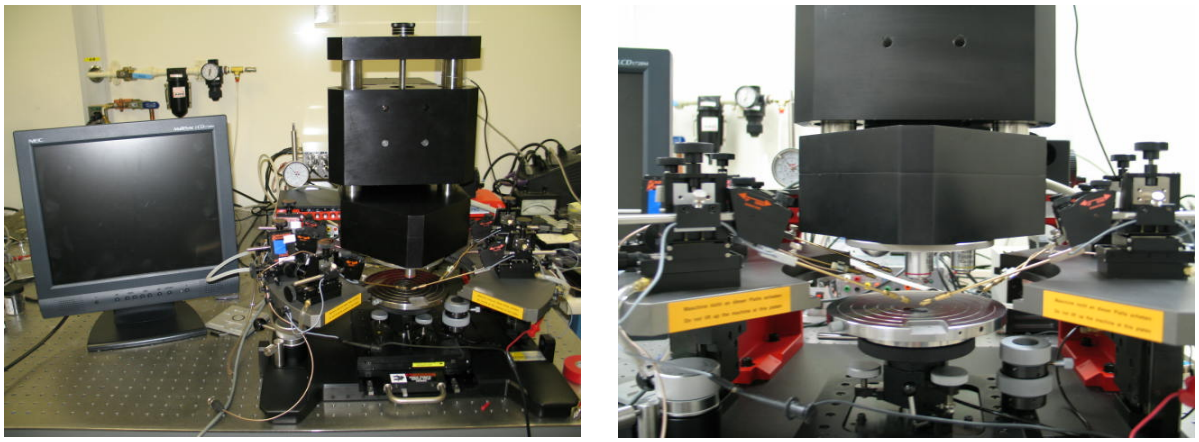


Figure 50. MEMS Motion Analyzer by Umech Technology (left); the probe areas (right)

The power for the heat actuators is about 5-10 volts and less than 10 mA. The pulse is around 5 msec. For a complete cycle of switching, it would need motion of driver actuator, opening of latching, and close of latching. Thus, the switching speed can be around several hundred hertz. Figure 51 shows a heat actuator that has been successfully actuated.

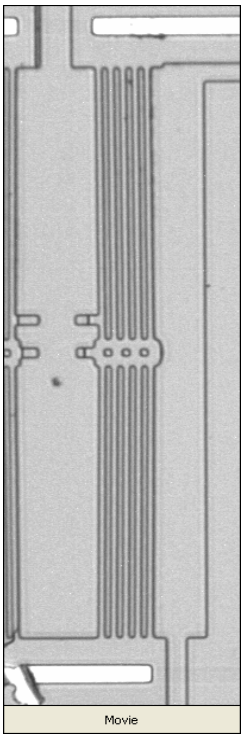


Figure 51. Heat actuator

The chip made by the optimized dry and wet etching technique at Infotonics has about 0.55 to 0.6 dB/cm optical loss, which is much better the same design made by another commercial MEMS foundry, 1.3 dB/cm. This, however, is not state-of-the-art. Additional wet etch and thermal smoothing methods will be examined. The heat actuator for the optical switch has been successfully actuated at 5 msec pulse. The motion analysis technique has been set up for up to 10 MHz capability.

The waveguide process is already being applied to new projects of interest to DoD and related agencies. In particular, Infotonics is subcontracting to Corning, Inc., on a project to develop an optical backplane interconnect for high speed computing (Figure 52). Silicon waveguides and AWGs similar to those in the ROADM will be used as optical multiplexers and demultiplexers that are index-matched to the Corning SOA's (semiconductor optical amplifiers) used to switch the signals on and off.

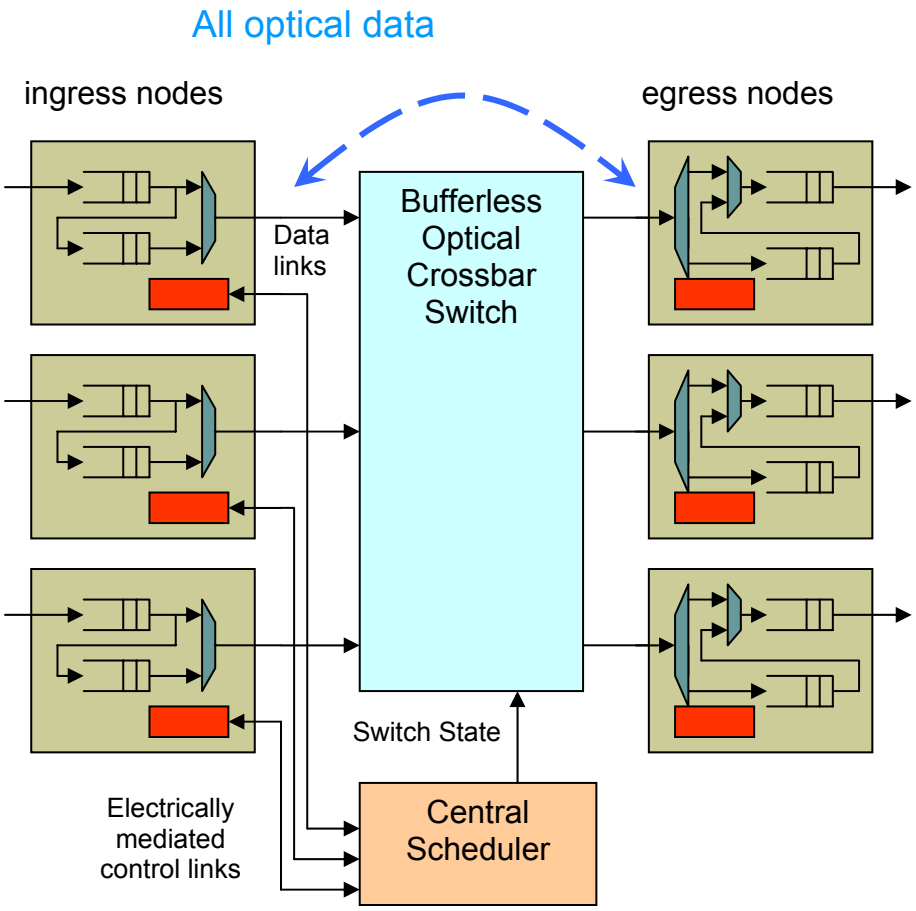


Figure 52. Schematic of Corning's high speed optical backplane interconnect.

6. Ring Laser Design, Fabrication, Characterization and Packaging Collaborative Project between: Infotonics Technology Center, Binoptics and AFRL-Rome

Infotonics collaborated with Binoptics and AFRL-Rome Labs to design, fabricate and package semiconductor ring lasers for photonic digital logic.

BinOptics Corporation has demonstrated the ability to design and fabricate semiconductor ring lasers having properties of interest for photonic digital logic and analog to digital conversion applications. In particular, the bi-stability of these devices allows them to be used as logic gates and comparators. In a study funded by ARFL-Rome, the speed characteristics of these lasers were investigated with promising results. It was shown in this work that the bidirectional semiconductor ring laser can invert signals at a speed of 10Gb/s and that these devices can be switched with very small injected powers in the region of 2μW. Great care must be taken in matching wavelength, polarization and injected pulse shape. These items become easier to control if the devise are monolithically integrated with other sources, which can be achieved with etched facet technology. The control of facet positions can also be utilized to reduce reflections, as facet angle does not have to be perpendicular to the cavity.

Speed is a key issue for ADC, and the interference of relaxation oscillations has been a concern. However, it has been shown that increasing current will increase relaxation frequency, and a shorter cavity will do the same. Another option is to increase the number of quantum wells in the structure, thereby increasing the gain. Relaxation frequency is proportional to the square root of the gain. Linear lasers have been made by BinOptics with relaxation frequencies above 15GHz, and much higher frequencies are possible. The injection of light will also increase the resonant frequency, but at the injection levels here, this should be a minimal change.

The above discussion assumes that the switching is effected through changes in the carrier density. Ideally, switching will be achieved by preferentially exciting one mode or the other by injection while keeping the carrier and photon densities the same. This process should be much faster than the carrier-related effects.

The next requirement on the way to building a photonic ADC is to fabricate more devices and characterize the ability to act as an accurate comparator. The devices measured in the initial study, showed the ability to switch, but the extinction ratio is a function of injected power. Methods to find a truly bi-stable device have been considered, and include, on one hand, trimming into balance and on the other the approach of an integrated mirror to make the device always lase in one direction.

In the past year a collaborative project was set up between Binoptics, Infotonics and AFRL-Rome. Binoptics role was to simulate, design and fabricate devices. Infotonics' role was to characterize and package the devices in order to provide a stable environment for testing. AFRL-Rome will test and characterize the devices more fully for specific applications.

Optoelectronic packaging is an expensive, time-consuming operation requiring great precision in the placement and alignment of components. The package design and implementation will affect the ultimate performance of the device significantly. Consideration must be made for mechanical support, thermal control, and electrical signal and power. To maximize the optical coupling between the device and the fibers, the fibers must be aligned using active feedback and placed with submicron precision. In order to package the ring lasers, we needed to do significant customization of packages to meet the specific fiber connection requirements. It is also imperative that the operating temperature of the laser be tightly controlled in order to control the output wavelength. For the ring lasers, there must be four fibers used for

input and output of the optical signals. Infotonics took on the task of designing, specifying, fabricating and integrating components to provide a suitable package for the ring laser devices.

Statement of Work

Binoptics continued the investigation of semiconductor diamond-shaped ring lasers through the design, simulation and testing of new devices with the objectives of demonstrating improved bi-stability, speed, and extinction ratios at high power. Binoptics fabricated a wafer containing several different design variables including etched trenches incorporated for more accurate dicing and improved coupling to fibers.

Binoptics used InP wafers with custom epitaxy to fabricate the devices, using more than 40 precision deposition, lithography, etching and characterization operations. The devices were characterized and singulated prior to packaging.

Twenty functional ring lasers were provided to Infotonics to package. The goal was to package the ring lasers and attach lensed fibers. The package was designed to maximize coupling, to provide stability in position of the fibers relative to the device, and to provide a stable operating environment, electrically and thermally. In this way, the devices can be more fully and repeatably investigated and characterized. It should also be possible to couple several of the devices together to show simple logic operation.

Work at Infotonics progressed in the following manner.

1. Initial Characterization of the ring laser parameters necessary for package design including far field profile, power, threshold current, and coupling parameters.
2. Design, and specification of ring laser package, and components.
3. Fabrication and procurement of components
4. Design and fabrication of laser welding fixture
5. Mounting of ring lasers on submount
6. Characterization of ring laser after placement on submount.
7. Stackup of components
8. Fiber Attachment for all four facets
9. Characterization of Final Packaged Device

The work content in each area will be reviewed in this report.

6.1 Initial Characterization of the Ring Laser Optical parameters

Ring laser devices from a prior run were characterized by Infotonics in order to understand the far field profile of the ring laser beam, the light power and spectrum of the output, and the coupling with lensed fibers. This information was used to design a package and specify components. An array of ring lasers, fabricated in 2003, was provided by Binoptics for initial testing to obtain information for package design.

Output Characterization:
Measurement of the output power and spectrum was performed by placing a detector as close as possible in the front of laser array as shown in the Figure 53, the distance between the detector and ring lasers was about 7 mm.

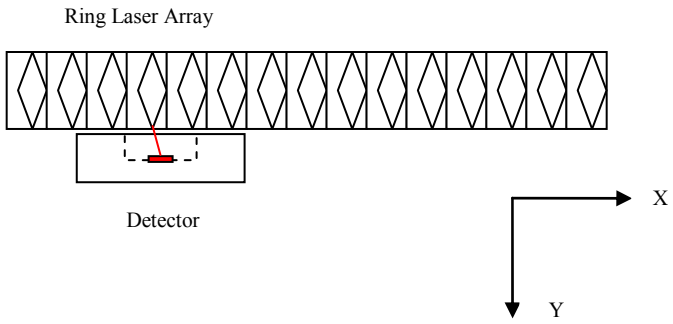


Figure 53. The sketch of the setup for power level measurement

The detector was shifted along the X and Z axes in order to obtain a maximum optical coupling power. During the measurement, the measurement of the light power meter was unstable, with fluctuations on the order of ± 10%.

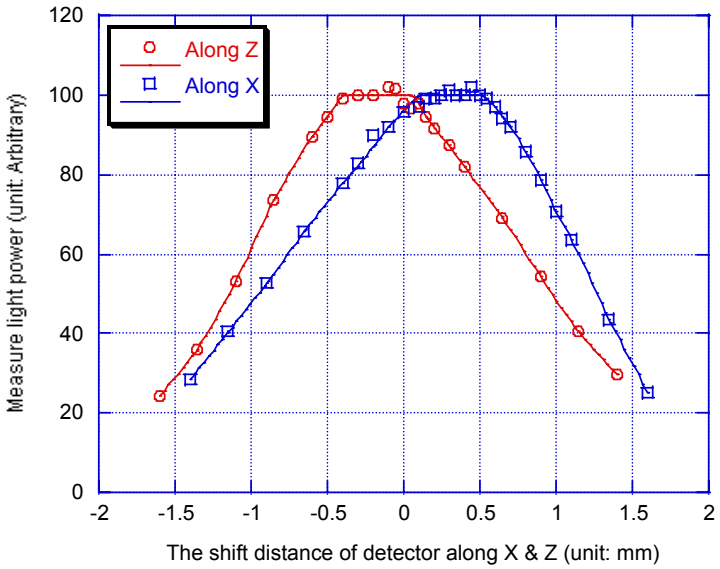


Figure 54. The light power verse detector position scanning along X & Z

The active area of the detector used is about 3 mm in diameter. Figure 54 shows two measured light power coupling curves plotted against the scanned detector positions along the X & Z axes. At the top of the power curves, there are flat areas. It indicates that the detector collects essentially 100% of the power of the beam when the detector was placed at the position indicated by the flattened region. The length of this flat area is about 400 □m long for curve scanning along X direction and is about 500 □m long for curve scanning along Z direction. This difference might be caused by relative position between detector and light beam. The detector is with an angle of 43° with the light beam in X direction, but is at a right angle with the light beam in Z direction. The light power curves in Figure 54 are not symmetric, which is consistent with the results of the BeamScan analysis, described and discussed later.

Based on the above discussion, it is possible to measure the light output versus diode current for one beam of the ring laser by placing the detector in front of the ring laser. Figure 3 shows the measurement results.

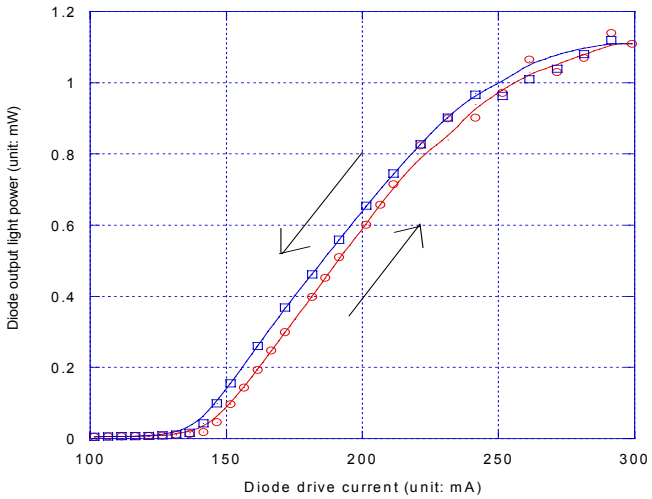


Figure 55. The light output versus diode current

The threshold current of this ring laser diode is about 140 mA, which is considered to be high (typical value is 50 ~ 100 mA range). The external efficiency for this ring laser is about 1 mW/mA x 4 ≅ 0.04 mW/mA (typical value is 0.05 ~ 0.1 mW/mA). The light power is saturated at 1.1 mW x 4 = 4.4 mW (typical value is 5 ~ 10 mW). Figure 56 shows the spectrum of the light with a peak at 1560 nm.

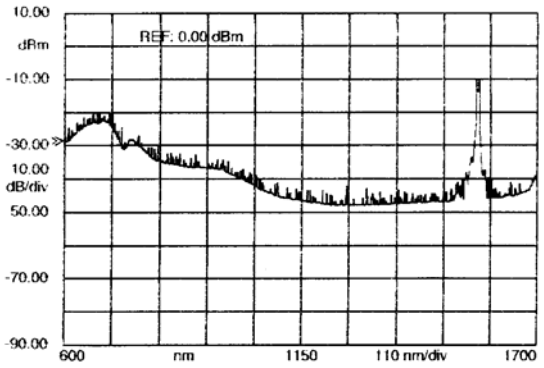


Figure 56. The spectrum of the laser light.

The Far-Field profile of ring laser beam

A BeamScan instrument, designed to profile laser beam size, uniformity and pointing angle was used to examine the output of the ring laser. The detector was placed in front of the ring laser with the detector position vertical to the laser beam. The measured result is shown in Figure 57.

The two dimensional profile indicates that the power peak is not at the center of the square beam. The X and Z power scan curves also show the non-symmetric nature of the power distribution. The widths of power curves at X and Z are almost the same with an average of about 3.6 mm. Since the distance

between the BeamScan detector and the ring laser is about 20 mm, the divergent angle of the laser beam is about 10° in both directions.

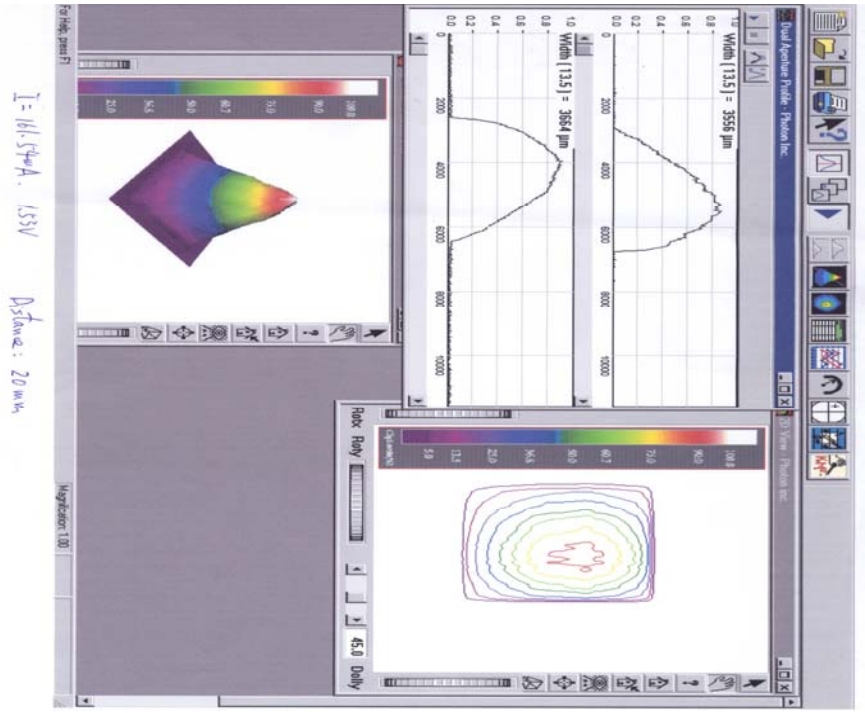


Figure 57: The far-field profile of laser beam by BeamScan

Measurement of Coupling with Lensed Fibers

The lensed fibers used in this test are standard Corning OptiFocus Lensed Fibers. The major specifications of these lensed fibers are listed in table 12.

Table 12: The specifications of standard Corning OptiFocus Lensed Fiber

OptiFocus Lensed fiber Specifications	Standard
MFD at Beam Waist ($1/e^2$ @ 1550 nm)	3.3 □m ± 0.3 □m
Distance to Beam Waist	> 20 □m
Far-field Divergence Angle θ_0 (FWHM @ 1550 nm)	20°
Fiber Type	SMF-28
Return Loss	> 40 dB @ 1550 nm
*Coupling Efficiency per Pair	85%

* Measured by coupling light from one lensed fiber into the other.

Two lensed fibers were mounted separately on micromanipulators. This allowed each lensed fiber to be placed in the optimum coupling position with one of the ring laser beams as shown in the Figure 58. The angle between the two coupled lensed fibers was 86°. The two lensed fibers were spliced with FC-PC connectors separately. The insertion loss during splicing was about 0.03 dB. Subsequently, the two lensed fibers were connected to HP 8616 light power meters.

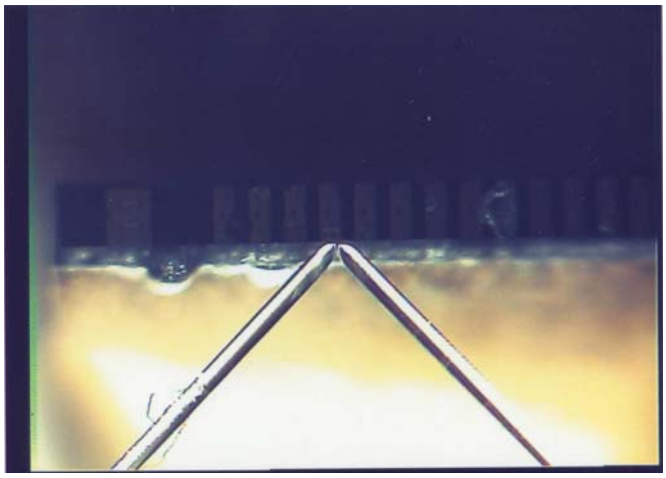


Figure 58. Micrograph of the lensed fibers coupled to the ring laser

Figure 59 shows the measured power from both lensed fibers measured simultaneously. In the current range from 100 to 210 mA, the light power levels from both lensed fibers were almost identical. After this limit the power levels of both lensed fibers diverged. The power level from lensed fiber 2 was much larger than that from lensed fiber 1. The light power from lensed fiber 2 was about 1.2 mW at the diode drive current of 300 mA. At the same time the light power from lensed fiber 1 was only about 0.7 mW. Both light power curves are largely **depart** when the diode drive current is larger than 220 mA. In Figure 57, only the average curve is similar to the light power curve shown in Figure 55.

As a result of these measurements, the Corning OptiFocus lenses with polarization maintaining fibers were chosen for the packaged device. The difference in the two fibers may be due to coupling or due to the difference in the performance of the device in the forward and reverse direction.

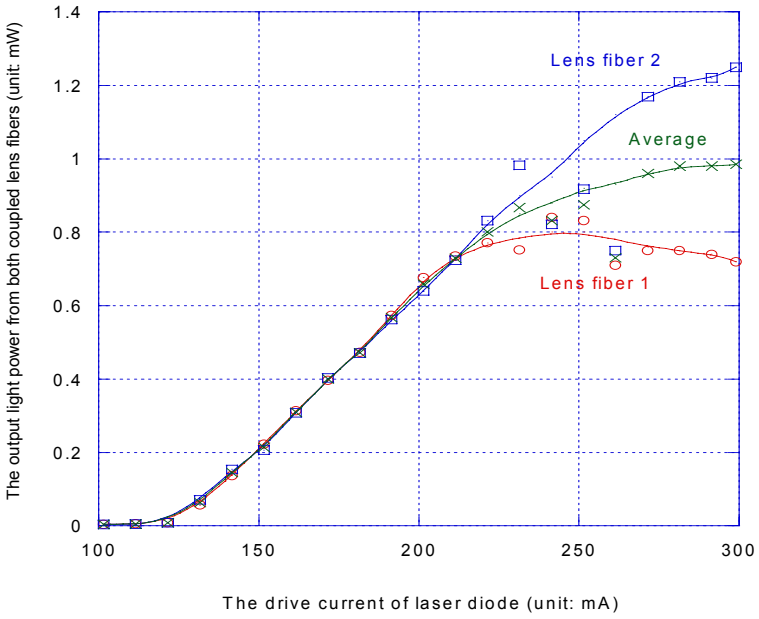


Figure 59. Plot of optical power from both coupled lensed fibers

6.2 Package Design

A ring laser package was designed with four fibers optical connections. The fiber specifications and spacing were chosen based upon the measurements and an analysis described below. Polarization maintaining fiber was chosen due to the device requirements. A thermoelectric cooler and thermistor were used to maintain the ring laser at its 25+/- 0.1°C. The operating current was 160 mA.

Generally optoelectronic packages are made using gold plated Kovar. The Kovar is chosen because of its dimensional stability. The gold plating allows solder connections of subcomponents to the base, and allows for hermetic sealing. The ring laser package would require a custom fabrication run due to its unusual requirements. These packages are expensive and have long lead times. In order to minimize cost and delay, we chose to modify an existing package. The drawings of the final package design are shown in Figures 60 & 61.

It was necessary to custom design a fixture for the Newport system laser welder to accommodate the ring laser design.

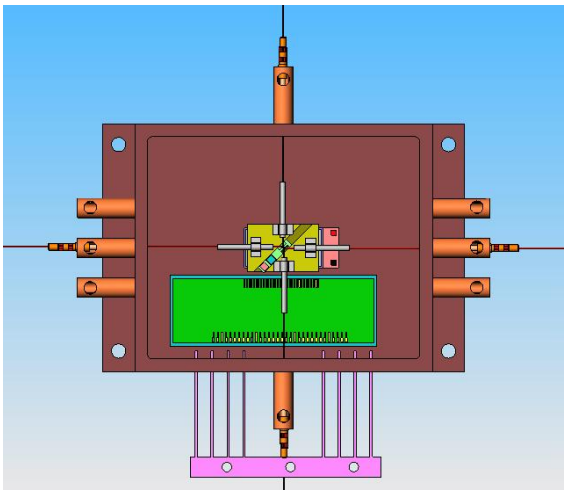


Figure 60: Drawing of Package Design for Ring Laser

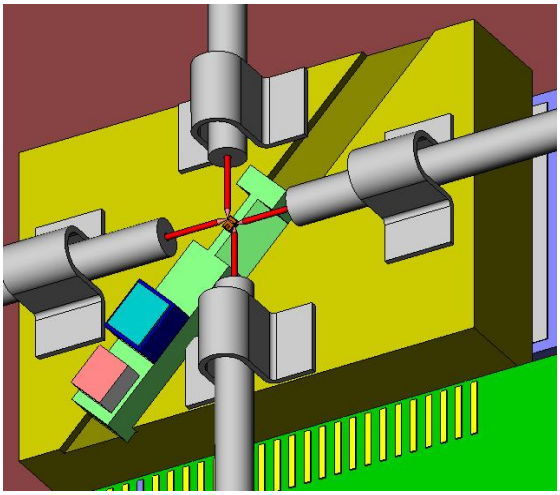


Figure 61: Blown up view of laser mounted on submount with ferrulized fiber connections.

Investigations into Design Parameters for Ring laser package

The placement and angle of the facets on the ring laser lead to severe challenges in fiber alignment. Normally, the fiber is placed quite close to the device facet, however the requirement to have both input and output fibers at each end of the diamond, means that the fibers must be placed so that they do not interfere with each other during packaging.

Basic parameters used for discussion:
The angle between two fibers coupling with the ring laser: 86°;
Basic specifications of the Corning OptiFocus lensed fiber, chosen for this package:

Wavelength (nm)	1550
Mode-field diameter at beam waist (□m)	3.3
Distance to beam waist (mm)	0.02

A picture of the lensed fiber has been acquired from Corning and is transferred to AutoCAD draw as shown in the following.

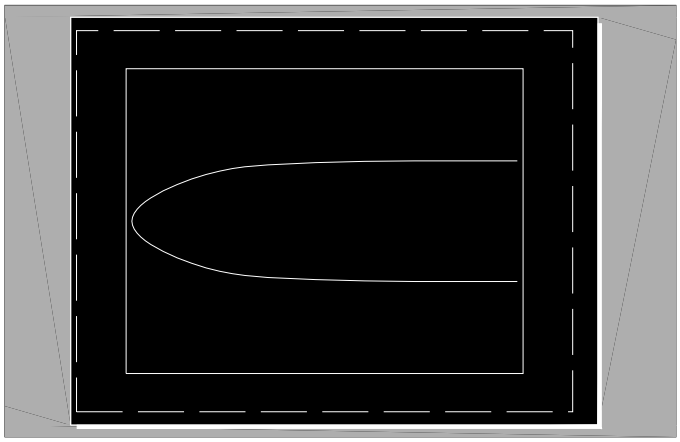


Figure 62. Lensed fiber

A major issue is the placement of the two fibers to allow maximum coupling and still avoid interference with each other through direct contact or interference) Placing two lens fibers contacting with each other and with an angle of 86°.

The result is shown in the following drawing with a distance of 8.2 □m from fiber tip to the cross-point of both center lines, which corresponds to the front side of the laser.

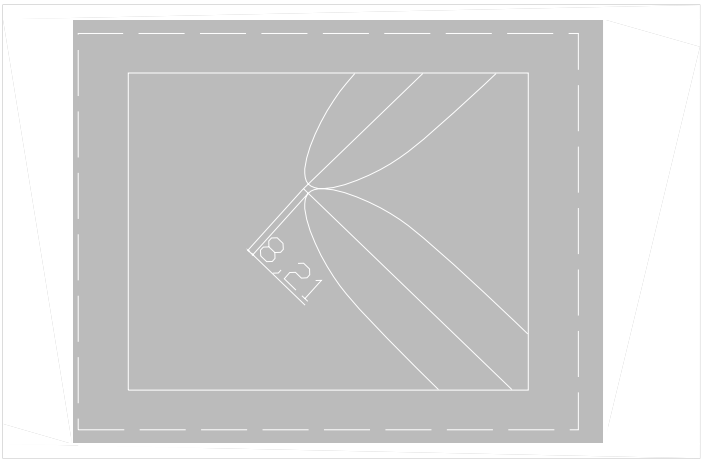


Figure 63. Placement of the fibers

When the distance from fiber tip to the cross-point is 20 □m, which is equal to the distance to beam waist of this lens fiber, the clearance between two lensed fibers is about 16 □m.

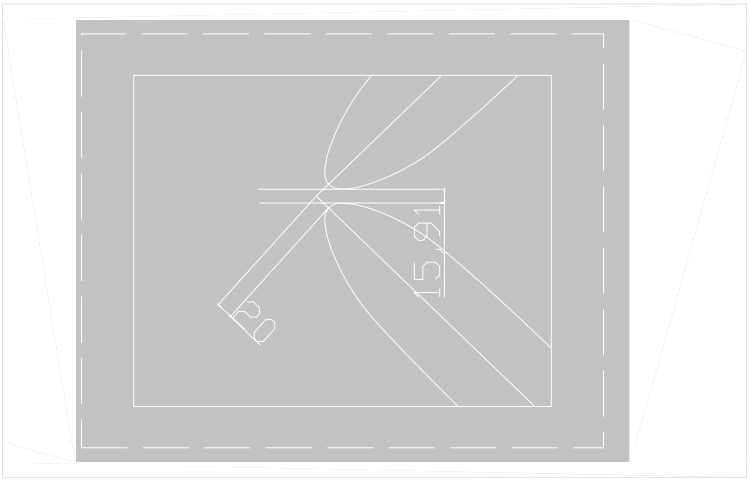


Figure 64. Placement of lensed fiber for optimum coupling

6.3 The measurement of Ring Laser Performance after Placement on Submount

After fabrication, the lasers from the fabrication run were attached to a submount and characterized. The submount was designed to allow close access of the fibers to the device, and still provide sufficient area for wire bonding and placement of the thermistor. The characterization was used to yield the die further assembly, and to provide primary data for alignment during laser welding. After fiber alignment, the performance of the laser could be compared to these values.

Figure 65 shows a sketch of the test system.

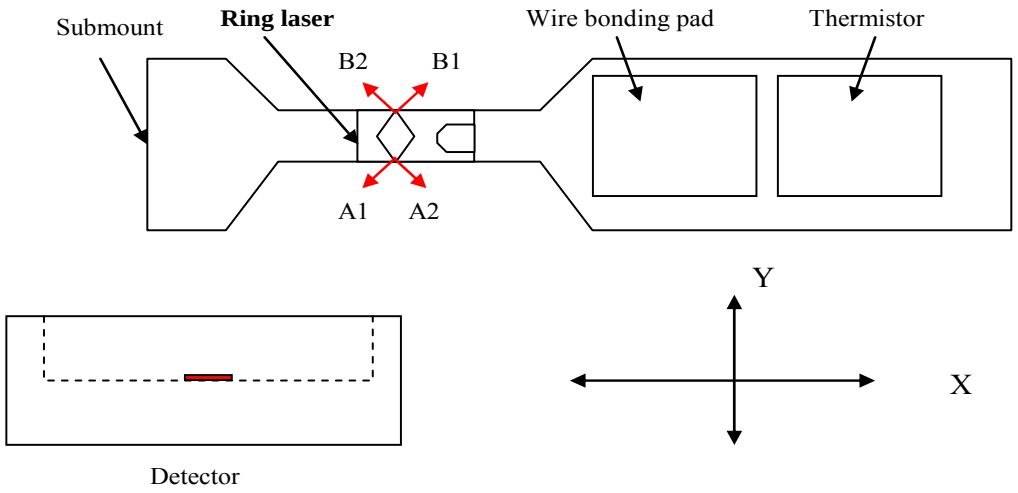


Figure 65. Sketch of the test system

The driving current (I) was applied to the ring laser through a probe. The detector, (3 mm in diameter,) was scanned along the X, Y, and Z directions to collect the light beam.. When the detector was set at a distance from the submount such as Y = 25 mm, two light peaks could be observed with the detector scanning along X direction. At the same time the photo intensity ratio of these two beams can be calculated (PI_{A1}/PI_{A2} or PI_{B1}/PI_{B2}). When the detector was moved as close as possible to the submount, the Y coordinate was about 13 mm. In this position only one broad peak was observed when the detector was scanned along the X axis. It is due to the overlap of two peaks as shown in Figure 66. The measured peak intensity of PI_{max} is larger than the peak intensity of each beam, but less than the summary of two peak intensities. The value of PI_{max} can provide a reference for the alignment between ring laser and lensed fiber. Figure 67 shows a typical curve of photo intensity versus ring laser diode current. After completing the A side measurement, the submount was rotated 180º in order to be measured in the B side.

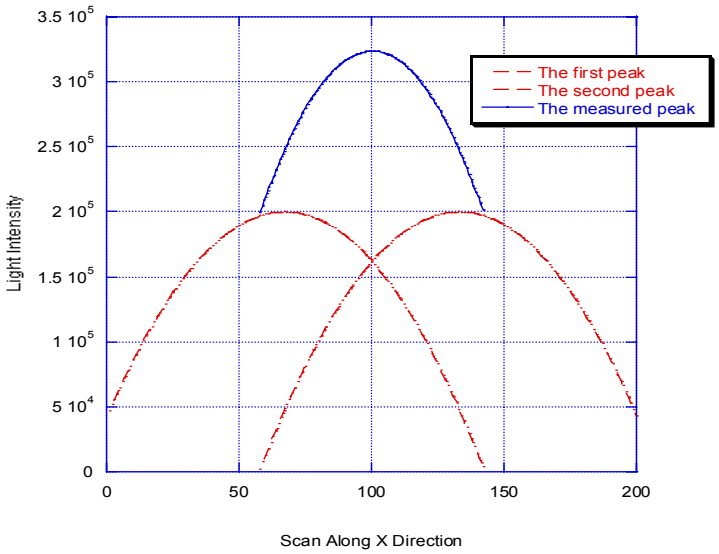


Figure 66. The measured peak is composed of two peaks.

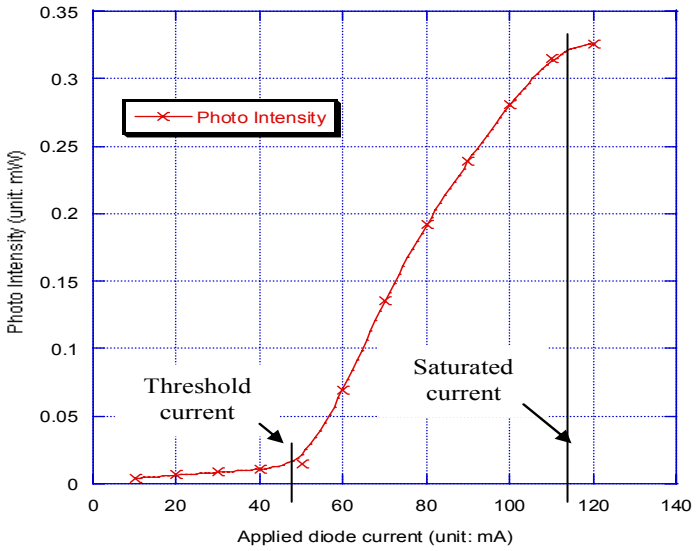


Figure 67. Photo intensity versus diode current

The following parameters have been measured during the test:

(1) The detector was located at the position with Y=25 mm to confirm the existing of two beams and to estimated PI_{A1}/PI_{A2} or PI_{B1}/PI_{B2}.
(2) The detector was located at the nearest position to determine the saturated current as shown in Figure 65 and the corresponding peak intensity PI_{max}.

Table 13: Results of Characterization after mounting ring lasers fabricated in Fall 2004, onto submounts.

Submount No.	Diode condition	A side				B side		
		Beam No.	PI_{A1}/PI_{A2}	Saturated current	PI_{max}	Beam No.	PI_{B1}/PI_{B2}	PI_{max}
1	Good	2	1/1	110 mA	0.20mW	2	1/1	0.25mW
2	Bad							
3	Good	2	1/1	120 mA	0.25mW	2	1/1	0.21mW
4	Good	2	¼	150 mA	0.43mW	2	1/2.5	0.42mW
5	Good	2	½	160 mA	0.58mW	2	1/1.5	0.59mW
6	Bad							
7	Bad							
8	Good	2	½	130 mA	0.17mW	2	1/2	0.13mW
9	Good	2	1/1	170 mA	0.63mW	2	1/1.5	0.63mW
10	Good	2	1.5/1	170 mA	0.63mW	2	1.5/1	0.63mW
11	Bad							
12	Good	2	1/1	140 mA	0.15mW	2	1/1.5	0.22mW
13	Good	2	1/1.5	160 mA	0.61mW	2	1/1.5	0.51mW
14	Good	2	1/1	180 mA	0.78mW	2	1/1	0.80mW
15	Good	2	1/1.5	160 mA	0.53mW	2	1/2.5	0.58mW

The results show that 4 of 15 were not “good” lasers after attachment to the submount. During the attachment of the ring laser to the submount, several issues arose. First it was difficult to work with parts as small as the ring laser and place them with the correct planarity and orientation. The placement was done with a manual die bonder. In the future we will utilize a flip chip bonder with micron-level placement. Secondly, wire bonding was difficult due to poor adhesion of the gold wire on the ring laser device. Examination of the data in Table 13 shows a variation in the relative strengths of the beams. When the ratio of PI_{A1}/PI_{A2} is equal to 1, it indicates the intensity of two beams is almost the same. When the ratio of PI_{A1}/PI_{A2} is equal to ¼, it indicates the intensity of A2 beam is four times of intensity of A1 beam. Since the detector is far away from the facet of ring laser (> 25 mm), the unequal intensity of these two beams is not caused by the reflection from the detector.

6.4 Fiber Alignment and Packaging Process

The submounts were placed in specially modified Kovar boxes, and fiber alignment was done utilizing a Newport 4200 fiber alignment system. Once the fiber was placed in the optimal position, the fiber was fixed in place by using a laser to weld a clip in place to the fiber and to the package. The fiber alignment was done for each fiber individually. After a stabilization bake, the fiber ports were sealed with gold-tin solder. A Kovar lid with a glass window was placed on top of the box and sealed.

Table 14 contains measurements taken for the final packaged devices, in this case Ring Laser #15. The placement of the device in the package is shown in the drawing in Figure 68. The infrared image of the device in Figure 69 is interesting. It shows loss of light on the sides of the ring laser away from the coupled facet.

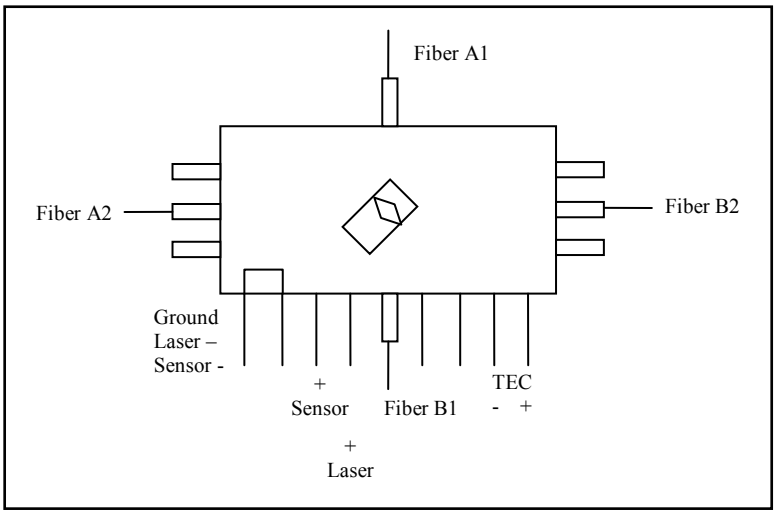


Figure 68. Placement of the ring laser in the package

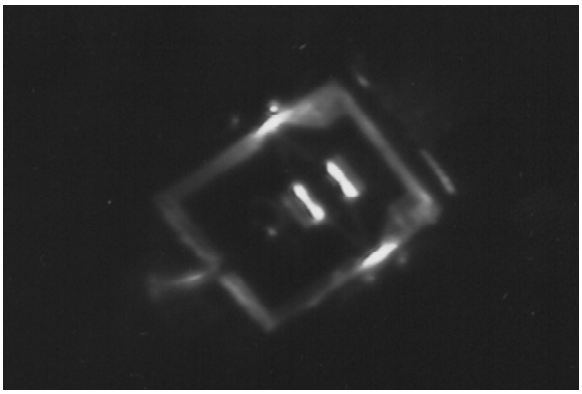


Figure 69. Infrared image of the ring laser #15

Table 14: Measurements of Packaged Ring Laser Device # 15

Fiber Channel	A1	B1	A2	B2
Output @ 25ºC @ Isat. Of 160 mA	0.44 mW	0.55 mW	0.44 mW	1.14 mW
RL	28 dB	31 dB	43 dB	42 dB
PDL	A1 → B1 2.1 dB B1 → A1 1.6 dB		A2 → B2 3.2 dB B2 → A2 2.8 dB	
Spectrum	1542.2 nm, 1543.8 nm, 1546.3 nm, 1550.5 nm			

Three packaged ring laser devices were provided to AFRL-Rome and to Binoptics in July of 2005. They are planning to characterize the device performance further.

7. Conclusions and Future Directions

Modern battlefield and conflict situations rely upon innovative technologies for success. Early optoelectronic device concepts promise to deliver just that. Integrating these with microsystem technology will equip existing and future weapons systems with superior functionality that enables such systems to prevail in the battlefield. Balancing the need for rapid field deployment with production of reliable and robust devices remains a significant challenge. The Infotonics Technology Center will provide the Air Force Research Lab with critical infrastructure and technical expertise to enable and accelerate the development of optoelectronic microsystem devices such as environmental, biological and chemical sensors, high speed communications, as well as other technology of particular interest to the Department of Defense. Infotonics, a partnership of industry, universities and government, operates as a national center of excellence to drive photonics and microsystems development and commercialization. One of the primary goals of the Center is to establish a unique, world-class research and development facility with a focus on manufacturability. A state-of-the-art microsystems prototype and pilot fabrication facility was established to enable rapid commercialization of new optoelectronic microsystem products. The Center has three primary areas of photonics and microsystems competency: device research and engineering, packaging and assembly, and prototype and pilot-scale fabrication. Center activities focus on next generation optical communication networks, advanced imaging and information sensors and systems, micro-fluidic systems, assembly and packaging technologies, and biomedical devices. Our

targeted university research, world class scientific and business staff, and state-of-the-art facilities was developed to provide key intelligent, cost-effective, and reliable technology and innovative elements to the DOD in support of its mission. We developed key processes to support the prototyping of innovative electronic devices.

In the first year, a state-of-the art MEMS fabrication facility has been designed and constructed for the development of MEMS and MOEMS devices for commercial applications of all types. It is capable of supporting silicon, metal, and polymer micromachining processes. A broadly enabling baseline process, the Foundation Process, has been transferred to Infotonics. This process is capable of running single- or multi-user designs which require single crystal silicon optical and mechanical structures and / or polysilicon-based micromachined mechanical structures. Infotonics' intentions for the Foundation Process in the future are not to offer it as a multi-user process, since so many compromises are required (for example the variations in CMP results with device type discussed in Section2), that optimum results are not available for any. Rather the process modules developed for the Foundation Process (e.g. deep silicon etching, low-stress polysilicon, silicon and oxide CMP, waveguide fabrication, etc.) will be applied on single device designs where required to achieve the desired device performance. Efforts are currently underway to make these process modules available to the outside through DARPA's MEMS Exchange.

Dry etching techniques for smooth waveguide sidewalls and optimum optical performance were developed. Three different techniques for measuring sidewall roughness were explored. The optical loss of waveguide for various sidewall roughness has been evaluated and correlated to the sidewall roughness by SEM pictures. For now SEM examination of waveguide sidewalls seems to be the best indicator of low loss. Efforts will continue to quantify roughness. Future efforts to improve the roughness measurements will include modification of the AFM to enable imaging of the sample to be measured in order to see where the measurement is taking place. As improvements are made in the SEM 3D imaging software, Infotonics will incorporate this method when appropriate. The Fabry-Perot loss measurement methodology will be used on future designs.

Additional work on specific devices of particular interest to the AFRL was pursued and substantial progress was made on the ROAD-M and ring laser devices that will help accelerate their deployment into field devices. These process and device technologies will be critical parts of systems that support and further DoD's "Future Warrior" program. Enabling high-speed agile flexible communication systems and high-speed optical communications as well as possible support for the Fly-By-Light program, they provide better flexibility, improved situational awareness, and facilitate informed tactical decision-making.

Infotonics proposed an integrated program to collaborate with the Air Force Research Lab to further DOD's mission. The research and development was broad based, including internal research and development of microfabrication and device packaging processes that enable prototyping the next generation sensor and optoelectronic devices here in the United States, providing an excellent source of trusted and assured quality. The proposed research and development activities undertaken during this project period will continue to provide significant value to our government sponsor in meeting both near term needs and for long term objectives.

PATENTS & INVENTIONS

None

PUBLICATIONS & PRESENTATIONS

Lin, P., Boysel, RM, Boysel, M, Winters, M., Hawkins, W., Kubby, J., Gulvin, P., Diehl, J., Feinberg, K., German, K., Herko, L., Jia, N., Ma, J., Nystrom, P., and Wang, YR. (2005) Multi-user Hybrid processing Platform for MEMS Devices Using Silicon-on-Insulator Wafer. MEMS 2005, Miami, FL

APPENDIX A. TECHNICAL STAFF

Scientists

Mark Boysel, ***Senior MEMS Scientist***

Mark has been working in the field of MEMS and microfabrication for 18 years. He received his Ph. D. degree in Experimental Low Temperature Condensed Matter Physics from The Ohio State University 1981. He held post-doctoral positions at Imperial College in London, and at the University of California, Santa Barbara under Alan Heeger, where he worked respectively on working on inhomogeneous superconductors and conducting polymers. From 1985-1995 Mark worked at Texas Instruments' Central Research Laboratories where he helped develop the Digital Micromirror metal surface micromachining (MEMS) technology used in TI's DLP (Digital Light Processing) projection televisions and in conference room and theater projectors. Since 1995 Mark has worked in three start-up efforts (eMagin, Motorola Flat Panel, and Solus Microtechnologies) to develop other display technologies including field emission displays and electron beam addressed MEMS and elastomeric displays. Prior to joining Infotonics, Mark managed the Surface Science and Nanotechnology Group in the Fundamental Research Division of Corning, Inc.

Jose Mir, ***Director-Biomedical Initiatives***

Jose began his professional career in 1974 working as a research physicist at the Eastman Kodak Research Labs. Jose's research at Kodak was quite diverse involving such areas as theoretical fluid mechanics, ceramics engineering, organometallic chemistry, photoelectrophoretic charge transfer, ultrasonic cavitation/atomization, superconductivity, integrated optics, MEMS, heteroepitaxial thin film growth, second harmonic generation, quantum optics, electrooptics, ferroelectrics, digital imaging systems design, ASIC circuit design, and more. He founded and led three new research laboratories that created new technologies commercialized in a number of Kodak products and manufacturing processes. Jose has over 70 US patents and scientific publications in refereed journals.

Upon the realization that science and technology were necessary but insufficient elements for business success, Jose shifted toward a hybrid business-technical career direction. In 1993 George Fisher, Kodak's new CEO, recruited Jose for his RONA (Return On Net Assets) initiative aimed at extracting greater value from Kodak technology. In this role, Jose worked with Kodak's businesses to understand and reengineer the end-to-end business process "light bulb to dollars". There were several deficiencies identified, most notably the need to fill a gap defining, incubating, and taking to market digital products. As a result, Jose was one of two Kodak executives chartered to create an incubator for high growth digital opportunities. The new division became a global innovation engine with staff of over 60 professionals with diverse backgrounds including science, engineering, business, finance, marketing, human factors, product design, and anthropology. Five years after its birth, the organization succeeded in providing Kodak a revenue pipeline in excess of $1B and over 600 patents. In his last major assignment at Kodak, Jose started and managed a new Kodak business serving the motion picture and television industries. In this capacity, Jose had full responsibility over business/technical strategies, P&L, and operations of a product portfolio exceeding $15M annual revenue. His business commercialized four radically new digital imaging product families, two of the products won awards for technical excellence at NAB 2001.

Jose left Kodak in 2004 to pursue entrepreneurial interests. He found an ideal environment at Infotonics Technology Center given its capabilities and mission for economic development through business development. Jose sees SpectralSight as a great opportunity to harness his energy, leadership, broad scientific knowledge, creativity, business skills, and entrepreneurship.

A native of Cuba, Jose earned a BS degree in Physics from the University of Miami in 1973 and also excelled in college as a competitive gymnast. Jose has won a number of awards such as the Kodak Distinguished Inventor Award, Hispanic Corporate Achievers 2000 Director of the Year National Award, and was Kodak's selection for 2001 HENA National Award. He has participated on the Board of Directors of a number of companies and universities.

Nancy Stoffel, ***Senior Scientist***

Nancy has 18 years of experience working on materials issues associated with microelectronics and electronic packaging. Her education includes a BS in Chemical Engineering from the University of Virginia, an MS in Chemical Engineering and Applied Chemistry from Columbia University, and a Ph D in Materials Science from Cornell University. Nancy's doctoral dissertation, under Professor Edward Kramer, explored the adhesion of polyimides from both a fundamental and practical viewpoint.

Nancy worked for IBM from 1984-1992 in their electronic packaging laboratory developing sintering processes for the co-fired glass-ceramic/copper multichip module. From 1995 to 2001 Nancy worked for Xerox in the inkjet business division. In this position she worked on development of polymeric materials for harsh environments, photopolymer synthesis and processing, adhesion optimization, wafer bonding, encapsulation, microwave processing, reliability, materials selection, failure analysis, accelerated testing and lifetime predictions. From 2001 through 2003, Nancy managed a group responsible for developing a die module and materials set for Fuji Xerox's next generation of products, and doing technology transfer to Japan.

Songsheng Tan, ***Research Scientist***

Songsheng is a scientist with extensive 30 + years of "hand-on" experience in the field of optoelectronics packaging, semiconductor processing, micromachining, MEMS, and materials science. He earned BS and MS in Metal Physics at University of Science and Technology of Beijing, China. He was a full professor at Shanghai Institute of Metallurgy, Chinese Academy of Science and Technology and worked at various projects including Micro Wobble motor, Micro magnetic floating rotor, Micro-resonator, Polycrystalline and Amorphous silicon pressure sensors, High temperature sapphire pressure sensors, Platinum thin film thermal sensors, Diamond film deposition by microwave CVD, etc.

In 1993 Songsheng was invited as visiting scholar at Carnegie-Mellon University . During this period he had cooperated with AMP to work on the development of Silicon Optical Bench with mechanical passive alignment (SiOB). His contribution in SiOB technology was to develop high speed SiOB up to 40 GHz. Later he joined AMP, Corning to work on various product development based on SiOB technology including bi-direction transceiver, Triplexer, EAM module, 8-channel tap device, integrated coupler tap, and so on. Since 1993 he has published 20 papers and has been award six US patents.

Dennis Zander, *Chief Scientist, Applications*

Currently Dennis is program manager for Infotonics' mini-hyperspectral imaging initiative. His prior experience as a Manager of New Business Development with the Production Systems Engineering and Technology Division of Eastman Kodak led to Kodak's landing a contract to develop and manufacture fuel cells for a leading fuel cell developer. In addition, he and a colleague uncovered a billion dollar opportunity for portable energy, which is currently under negotiation. Prior to that, Dennis was Head of Advanced Camera Development for Consumer Imaging Cameras. He directed the development of two generations of new cameras with unique additional features in each successive generation. During his tenure as a Lab head in Research, he led a group of 50 Ph.D. scientists, engineers, and technicians who

collaborated to integrate materials development, manufacturing process development, and product design. As a Senior Product Engineer with Kodak, he lead the team that designed the new APS film cartridge and before that lead a team that developed manufacturing processes and product design of PCR pouches for DNA amplification that were part of the Clinical Products Division purchased by Johnson & Johnson. In his time at Kodak, Dennis received over 90 patents in every area of business in which he worked. On his own time, Dennis was a partner and major contributor to two software companies, one for computer game software and one for educational software. More recently, he has started his own company, Z-Stuff for Trains, that designs and sells accessories for model trains. In that role, he has developed and patented 10 new products, several setting new standards for the industry.

Pinyen Lin, ***Senior MEMS Engineer***

Pinyen has been involved in the development of microfabrication process and material characterization for microsystems for over 10 years. He received his Ph.D. degree in Materials Science and Engineering at M.I.T. in 1991, under Professor Stephen Senturia, with the study in the in-situ measurement of mechanical properties of multi-layered thin films on silicone wafers.

Pinyen is a member of research staff of the MEMS group at Xerox Wilson Center for Research and Technology. His current assignments include the setup and optimization of fabrication equipment at ITC as part of contributions from Xerox, one of the founding members of ITC. Pinyen has extensive working experience in many microfabrication facilities including Cornell NanoScale Facility (CNF), Microsystems Technology Laboratories (MTL) at M.I.T., and Semiconductor & Microsystems Fabrication Laboratories (SMFL) at Rochester Institute of Technology. He has worked on various projects in design, fabrication and packaging of microsystem devices such as microfluidic dispensers and channels, resonators, optical switches, and optical add/drop modulators (OADM). He has received the Xerox Team Excellence Award in 1995 and holds sixteen U.S. Patents.

Fabrication

Mary Boysel, ***Fabrication Manager***

Mary has nearly 20 years of microfabrication experience over a broad range of applications in MEMS and semiconductors, including telecom devices, flat panel displays (field emission, micromirror, and liquid crystal), and analog and digital microelectronics. She has worked in a variety of technical environments including high volume manufacturing (Allegro MicroSystems) as well as research and development (Raytheon and Motorola). Mary earned a Bachelor of Science degree at the University of Wisconsin and has performed technical management in microfabrication for nearly 15 years. Experienced in three start-up operations, Mary defined the processes, equipment, facilities, and personnel requirements to bring the ITC fab on line.

Mark Scholefield, ***Senior Process Engineer***

Mark has over 20 years experience in the semiconductor industry, working at Agere Systems, Lucent Technologies, AT&T, and National Semiconductor. Currently, he is responsible for all diffusion and LPCVD processes at Infotonics. Working extensively in bipolar, CMOS, and BiCMOS integrated circuit manufacturing, he has substantial experience in APCVD, LPCVD, PECVD of thin films for integrated circuit and optoelectronic device manufacturing and development. In 2000, he transferred to the optoelectronics business unit of Lucent Technologies where he helped scale up processes for the manufacture of silica waveguides, lithium niobate modulators, and indium phosphide lasers and detectors. Mark received his B.S. degree in Chemical Engineering from the University of Massachusetts at Amherst in 1983.

Mary Winters, ***Senior Process Engineer***

Mary has been working in the MEMS field for 8 years. She has a B.S. degree in Chemical Engineering from the University of Rochester and a M.E. degree, specializing in MEMS from the University of Illinois. Mary comes from Eastman Kodak where she was a Senior Development Engineer. While at Kodak, Mary worked on developing reflective films for conformal grating electromechanical devices, dielectric and anisoptropic polyimide dry etch processes for inkjet devices, dielectric dry etch processes for organic cavity lasers and ion implantation surface modification techniques for molding titania-based lenses. In graduate school, she studied the effects of mass absorption on microcantilever beams and during undergraduate she designed and tested microchannel membranes to study how physical forces, such as pressure and flow within arteriolar microcirculation, affect endothelial cell function.

Roger Kovalec, ***Process Engineer***

A photolithography and wet etch engineer who worked at Agere Systems, Anadigics, Canon USA, and Harris Semiconductor, Roger brings over 15 years of experience in wafer fabrication to Infotonics. His processing experience includes work on III-V materials (gallium arsenide, indium phosphide) as well as silicon substrates, using spin-on dielectrics, polyimides, in addition to photosensitive novalak resins for patterning. Process development, optimization, and trouble-shooting have been demonstrated by Roger through methods such as designed experiments and statistical process control and comes from an ISO/Total Quality Management environment.

Jennifer Laemlein, ***CMP Process Engineer***

Jennifer comes to ITC after working for 4 years with Ferro Electronic Materials (manufacturer of CMP slurries). In her role at Ferro, she advised CMP users on processing (oxide and polysilicon CMP) and various post-CMP cleaning methodologies for process optimization. With a Bachelor of Science degree in Chemistry, she combines the theory and hardware in practical application with a methodical problem solving approach.

Judy Sline, ***Metrology Technician***

Judy has over 20 years of manufacturing and process development experience, focusing on product quality assurance and process improvement at both small startups (Guardian Industries) to large corporations (Xerox and Philips/GTE). Experienced in developing and implementing quality plans including lab procedures, product compliance matrices, and work instruction to insure product quality and consistency, she utilized optical microscopy, SEM, EDS, and FTIR to identify root cause of product contamination and defects to drive corrective action, yield improvement, and assure quality and reliability. While at Xerox, Judy was recognized by management over 15 times for solving critical program problems and improving yield. She has been awarded eight U.S. patents.

David Gallipeau, ***Process Engineer***

Having worked at Veeco Instruments on high vacuum deposition equipment for over 4 years, David is responsible for the sputter deposition (DC, Rf), e-beam metal evaporation, and dielectric evaporation toolsets. His experience on both the hardware and processing aspects of thin film deposition has honed his trouble-shooting skills for development and optimization of new processes. Through Six Sigma methodologies, ISO procedures, statistical process controls, and Taguchi methods, he was recognized for his dedication to excellence at Veeco Instruments with the Team Excellence Award in 1999 as well as the Outstanding Performer Award in 1998 and twice in 2000.

Diane Atkinson, ***Process Technician***

With over 20 years experience in a microfabrication R&D environment (Xerox, Kodak), Diane's polymeric expertise includes SU-8, polyimide, multi-layer, and novel photopolymeric resin processing. She has demonstrated performance in process characterization and development in film adhesion, patterning, development, and mechanical and reliability testing. Her skillset includes use of Mat Lab and Lab View. Diane has been recognized with Xerox's Achievement in Science and Technology Award and has noted for her contribution on several Xerox patents.

Maintenance Team

On average, the maintenance team brings 20+ years of experience to bear in maximizing tool availability while minimizing tool cost. This is due to creativity (many specialty tools are designed in-house and machined locally), experience with specific tooling (trouble-shooting of familiar equipment), maturity, an appreciation for preventative maintenance, and a solid methodology in problem solving.

Doug Stewart, ***Senior Equipment Maintenance Engineer/Supervisor***

22 years semiconductor maintenance and equipment engineering activities, working at Eastman Kodak Company, Xerox Corporation, and National Semiconductor Corporation, gives the maintenance team a solid resource on which to draw. While an expert in high vacuum system, his skills include trouble-shooting hardware and process problems to equipment evaluation, selection, facilitization, modification, and on-going maintenance over a wide variety of tools.

Jim White, ***Equipment Maintenance Technician***

37 years experience in machine design, hydraulics, pneumatics, and robotics at Eastman Kodak have proven extremely useful in bringing the ITC tooling on-line. In addition to this, Jim's AutoCAD and SolidWorks capability allow ITC the specialty fixturing/tooling required to design and fabricate novel assemblies. Jim has 16 patents associated with his work done at Kodak.

Lerry Schaftlein, ***Equipment Maintenance Technician***

With 15+ years experience with Philips Semiconductor and Semifab Inc. in semiconductor equipment repair, maintenance, installation, and improvements/upgrades, Lerry offers an in-depth expertise in photolithography and wet chemistry toolsets backed with solid all-around mechanical and electrical training.

Bob Welch, *Equipment Maintenance Technician*

31 years of experience at Eastman Kodak Company and Harris Inc. Although Bob's area of expertise is plasma and high vacuum systems, his training includes electrical, mechanical, and engineering design.

Jim Duncan, *Equipment Maintenance Technician*

6 years experience in semiconductor tooling manufacturing at JST Manufacturing, SCP Global Technologies, and manufacturing at Micron Technologies, Jim has worked robotic, pneumatic, hydraulic, and sensing technologies problems. His training has included electrical, mechanical, and test equipment and has proven his capabilities at ITC.

Packaging*

Almon Fisher, ***Packaging Engineer***

With 21 years of experience, Al is a R&D materials process engineer with extensive experience in microfluidic MEMS technology including process development and manufacturing support, microelectronic & MEMS packaging, and material selection and testing. He received his B.S. in Chemistry and M.S. in Material Science from the Rochester Institute of Science. Al has 26 patents in magnetography, inkjet, CMP, filtration, photolithographic polymers and dicing technologies.

Chuck Shick, ***Packaging Technician***

Chuck brings his 15+ years experience in precision engineering on a manufacturing team to Infotonics' packaging facility. He worked at Xerox Corporation, Corning Incorporated, Bausch and Lomb, Pulsafeeder Inc., and Eastman Kodak Company in positions of increasing responsibility for precision motion control systems that utilized his strong precision mechanical, instrumentation and metrology skills. In his most recent position, he worked closely with design engineers and scientists to develop experiments and tests to determine design performance and reliability of thermal and solid inkjet print heads.

* Infotonics currently leverages in-kind Kodak support through use of their packaging facility and personnel. Plans to renovate and locate the packaging lab here at Infotonics are underway for 2005.

APPENDIX B. MICROFABRICATION AND DEVICE PACKAGING AVAILABLE TECHNOLOGIES & PROCESSES

A. MICROFABRICATION TOOLS AND PROCESSES

Device Technologies

- Microoptic/Photonics
- Microfluidic
- Mechanical

Microfabrication Processes

- Furnace
  - * LPCVD nitride, poly, wet/dry oxidations, TEOS, PSG, BPSG, POCl3 doping, anneal
- PECVD
  - * TEOS, doped/undoped SiO2, silicon nitride, silicon oxynitride, germania, dep-etch
- Metal Sputter/evaporation
  - * Cr, Au, Al,Al alloys, W, Ti, TiW, custom
  - * Reactive metal oxide deposition (silica, titania, tantala, alumina)
- Plasma Etch/RIE
  - * DRIE (Deep Reactive Ion Etch): Si, SiO2
  - * RIE (Reactive Ion Etch): Si,polysilicon, oxide nitride, metal, polymer
  - * Photoresist strip/descum
- Wet Processing
  - * Wet cleans (acid & solvent)
  - * Wet etches, including Hot H3PO4, KOH, BOE
  - * Lift-off
- Photolithography
  - * Coat/Develop/Cure: Positive, negative resist, SU-8, polyimide
  - * High-res stepper (0.5 μm)
  - * Large field 1x stepper with backside alignment
  - * Contact aligner with backside alignment
- Additional Processes

* HF vapor, XeF2 releases
* Wafer bonding
* Chem-mechanical polish
* Wafer grind
* Parylene CVD Substrates
  - * Silicon, SOI, glass, quartz

B. DEVICE PACKAGING

Technologies

- Planar optic packaging
- Optical fiber pigtailing and alignment
- Silicon optical bench
- Free space optical
- Electro-optic
- Microfluidic
- Electronic

Tools and Processes

- Microassembly
  - * Wafer scale bonding

* Silicon optical bench
* 3D packaging

- ❖ Wafer/Singulation
  * Dicing
  * Scribing (mechanical and laser)
  * Cleaving
- ❖ Adhesive dispensing
  * Precise volume and position
  * Ultra small volume pin transfer
- ❖ Die placement
  * Precision pick and place
  * Flip Chip
  * Eutectic bonding
- ❖ Fiber attach
  * Laser weld
  * Optical adhesives
- ❖ Interconnect
  * Thermal gold ball wirebonding
  * Aluminum wedge wirebonding
  * Pigtailing
- ❖ Optical fiber alignment
  * Active alignment ind. fibers/fiber arrays
  * Passive alignment w/ silicon optical bench techniques
  * Dual fiber pigtail packages
- ❖ Package sealing
  * Custom packages
  * Hermetic packaging
  * Glass bond
  * Laser weld
  * Seam sealer

C. TEST AND METROLOGY

<u>Process Metrology</u>

- ❖ Scanning electron microscopy
- ❖ Atomic force microscopy
- ❖ Contact profilometry
- ❖ Optical film thickness measurement
- ❖ Wafer bow
- ❖ Static and dynamic interference profilometry
- ❖ Ellipsometry
- ❖ Resistivity profiling
- ❖ Electrical probing
- ❖ Optical microscopy
- ❖ Dynamic mechanical analyzer

<u>Measurements</u>

- ❖ Optical measurement/characterization
- ❖ Coupling efficiency
- ❖ Optical gain
- ❖ Polarization dependent gain
- ❖ Saturation power

- Noise figure
- Hermeticity/leak test
- Geometric measurements
- Electrical test
- Environmental testing
- Bond strengths